

(19)



Europäisches Patentamt

European Patent Office

Office européen des brevets



(11)

EP 0 694 804 A2

(12)

EUROPEAN PATENT APPLICATION

(43) Date of publication:
31.01.1996 Bulletin 1996/05

(51) Int. Cl.⁶: **G02F 1/136**, H01L 21/84

(21) Application number: **95111765.4**

(22) Date of filing: **26.07.1995**

(84) Designated Contracting States:
DE FR GB

(30) Priority: **27.07.1994 JP 175113/94**
24.08.1994 JP 199388/94

(71) Applicant: **HITACHI, LTD.**
Chiyoda-ku, Tokyo 101 (JP)

(72) Inventors:
• **Ono, Kikuo**
Naka-gun, Ibaraki 311-01 (JP)
• **Tsumura, Makoto**
Hitachi-shi, Ibaraki 316 (JP)
• **Ogawa, Kazuhiro**
Mobara-shi, Chiba 297 (JP)
• **Sakuta, Hiroki**
Mobara-shi, Chiba 297 (JP)

• **Suzuki, Masahiko**
Mobara-shi, Chiba 297 (JP)
• **Kaneko, Toshiki**
Chiba-shi, Chiba 267 (JP)
• **Nakayoshi, Yoshiaki**
Mobara-shi, Chiba 297 (JP)
• **Onisawa, Kenichi**
Hitachinaka-shi, Ibaraki 312 (JP)
• **Hashimoto, Kenichi**
Hitachinaka-shi, Ibaraki 312 (JP)
• **Minemura, Tetsuro**
Hitachioota-shi, Ibaraki 313 (JP)

(74) Representative: **Patentanwälte**
Beetz - Timpe - Siegfried
Schmitt-Fumian - Mayr
D-80538 München (DE)

(54) **Liquid crystal display apparatus, semiconductor devices, and manufacturing methods therefor**

(57) The invention relates to a bright image liquid crystal display apparatus, a semiconductor device and a manufacturing method therefor.

The apparatus comprises gate lines (GL) formed on a substrate (SUB1) and an insulating film formed on the substrate, data lines (DL) formed so as to cross the gate lines, thin film transistors (TFTs) formed at the respective intersections of the gate lines with the data lines, and pixel electrodes (IT01) connected to the TFTs, wherein the central portion of the pixel electrodes is in contact with the substrate (SUB1) or the insulating film, and the peripheral portion of the pixel electrode is in contact with an insulating film which was the same layer as the gate insulating film (GI) of the (TFT). The end portion of the gate electrode of the TFT is tapered with a taper angle equal to or less than three times the taper angle at the end portion of the semiconductor pattern.

EP 0 694 804 A2

Description

Background of the Invention

(1) Field of the Invention:

The present invention relates to active matrix drive type liquid crystal display apparatus using thin film transistors (TFTs), semiconductor devices and manufacturing methods therefor.

(2) Description of the Prior Art:

In an active matrix type liquid crystal display apparatus, switching elements are provided corresponding to respective of a plurality of pixel electrodes arranged in a matrix. In the active matrix type liquid crystal display apparatus, the liquid crystal at the respective pixel is always driven theoretically, and the contrast is higher than that of a simple matrix type display apparatus which uses a time division drive system. Therefore, the active matrix type technology is indispensable, especially for color displays.

In accordance with the prior art of the active matrix type liquid crystal display apparatus, the thin film transistors (TFTs) comprise an insulating transparent substrate, whereon a gate electrode (gate line), a gate insulating film, a semiconductor layer, a drain electrode (data line), and a source electrode are provided in that order. Transparent electrodes are connected to the source electrode. The structure of a TFT wherein gate electrodes are formed first on the substrate is generally called an inverted staggered structure. JP-A-61-161764 (1986) disclosed such a TFT.

Liquid crystal display apparatus using TFTs have high contrast because of the capability of active drive. However, the process for forming a TFT on the substrate is complex, and generally requires six or more photolithographic process steps (hereinafter called photo-treatment). When the number of photo-treatment steps for manufacturing the TFT substrate is large, there are problems in that the manufacturing cost of the TFT substrate increases, and further, the production yield of the manufacturing process decreases because of contamination with dust which comes from outside or is generated during the manufacturing process.

According to one of the prior art methods for simplifying the process, a gate insulating film and a semiconductor layer, and a metallic film to form the drain and source electrodes are formed continuously, the semiconductor layer is manufactured as a mask for the metallic film, and subsequently, transparent electrodes are formed.

However, this process involves the problem that the transparent electrodes are readily broken by a step which is formed by a remaining eaves-shaped end portion of the source electrode if the etching speed of the metallic film for the source electrodes is lower than the etching speed of the semiconductor layer. That means,

the production yield of the TFT substrates has not been considered sufficiently.

In order to realize a bright display image, the area of the light transmitting portion of the transparent pixel electrode (hereinafter called aperture ratio) must be as large as possible. However, in accordance with the above prior art, an increase of the aperture ratio for realizing a bright display image has not been considered sufficiently.

Further, at the ride over portion of the gate electrode in the TFT semiconductor pattern, a breakage may be generated in the semiconductor pattern because the end portion of the semiconductor pattern has a faster etching speed than the flat plain portion, and the electric leak current between the semiconductor layer and the gate electrodes increases. Accordingly, it has been a problem that a short circuit (G/D short) among the source electrodes, the drain electrodes, and the gate electrodes which are formed on the semiconductor pattern is readily generated.

Summary of the Invention

(1) Objects of the Invention:

One of the objects of the present invention is to provide a manufacturing method for an active matrix type liquid crystal display apparatus with less steps of the manufacturing process and a high production yield.

A further object of the present invention is to provide an active matrix type liquid crystal display apparatus capable of achieving a bright display image, and corresponding semiconductor devices.

Furthermore, it is an object of the present invention to provide a TFT substrate having an electrode structure capable of solving the above short circuit problem, and a liquid crystal display apparatus using that TFT substrate.

The above objects are achieved according to the independent claims. The dependent claims relate to preferred embodiments of the concept of the present invention.

(2) Solutions of these problems:

Step 1: A liquid crystal display apparatus is provided comprising a plurality of gate lines formed on a substrate, a plurality of data lines formed so as to cross the plurality of the gate lines, thin film transistors formed in the vicinity of the respective intersections of the gate lines with the data lines, and pixel electrodes connected to the thin film transistors, and having the function to drive the liquid crystal through the pixel electrodes, wherein the central portion of the pixel electrodes was made to be in contact directly with the substrate, and the peripheral portion of the pixel electrodes was made to be in contact with an insulating film which was the same layer as

the gate insulating film the thin film transistor is composed of.

Step 2: In the above step 1, a conductive film composing the pixel electrode was extended to the source electrode of the thin film transistor, and the contours in the plain pattern of the conductive film forming the source electrode were made to cross over the contours in the plain pattern at the region of the central portion of the pixel electrode being in contact with the substrate.

Step 3: In the above step 1, a light shielding film, which is in parallel with the data lines, and is separated and insulated from the data lines by an insulating film which was the same layer as the gate insulating film forming the thin film transistor, was provided between the data line and a region being in contact with the substrate at the central portion of the pixel electrode.

Step 4: In the above step 1, electric conductive lines, which correspond to respective of the plurality of gate lines and are in parallel to the gate lines, were provided, and capacitor elements were formed by providing an insulating film between the electric conductive line and the pixel electrode.

Step 5: A liquid crystal display apparatus is provided comprising a plurality of gate lines formed on a substrate, a plurality of data lines formed so as to cross the plurality of the gate lines, thin film transistors formed in the vicinity of the respective intersections of the gate lines with the data lines, pixel electrodes connected to the thin film transistors, and storage capacitors connected to the pixel electrodes, and having the function to drive the liquid crystal through the pixel electrodes, wherein the thin film transistor has a structure forming a gate insulating film on a gate electrode which was composed of a part of the gate line, a semiconductor layer on the gate insulating film, and a source electrode and a drain electrode on the semiconductor layer, an electric conductive film forming the pixel electrode extending to the source electrode, and the storage capacitor had a structure forming an insulating film which is the same layer as the gate insulating film on the gate line adjacent to the gate line whereon the thin film transistor was formed, and an electric conductive film which was extended from the pixel electrode on the insulating film.

Step 6: In the above step 5, the taper angle formed by the gate insulating film forming the thin film transistor with the substrate at the end portion of the semiconductor layer was made larger than the taper angle formed by the gate insulating film forming the thin film transistor with the substrate at the end portion of the insulating film forming the storage capacitor.

Step 7: In the above step 5, the source electrode was made to contact with the semiconductor layer, the gate insulating film, and the substrate.

Step 8: In the above step 5, the plurality of the data lines comprising semiconductors, and the electric conductive film forming the source electrodes and the drain electrodes, and the above members were placed in the same plain pattern.

Step 9: In the above step 5, the gate lines were coated, with an anodic oxide film of the electric conductive film forming the gate line.

Step 10: A manufacturing method for liquid crystal display apparatus comprising a plurality of gate lines formed on a substrate, a plurality of data lines formed so as to cross the gate lines, thin film transistors formed in the vicinity of the respective intersections of the gate lines with the data lines, and pixel electrodes connected to the thin film transistor, and having the function to drive the liquid crystal through the pixel electrodes, comprises the steps of etching both the gate insulating film and the semiconductor layer formed on the gate insulating film in the same process with approximately the same plain pattern, and subsequently, etching selectively the semiconductor layer.

Step 11: In the above step 10, a metallic film of a given pattern was formed on the semiconductor layer after etching the gate insulating film and the semiconductor layer in the same process, and subsequently the semiconductor layer was etched using the metallic film as a mask.

Step 12: In the above step 10, a process for anodizing the surface of the gate lines was further provided.

Step 13: In the above step 10, sulfur hexafluoride was used as an etching gas in the process of etching the gate insulating film and the semiconductor layer in the same process.

Step 14: In the above step 10, a mixed gas of sulfur hexafluoride and chlorine was used as an etching gas in the process of etching the semiconductor layer using the metallic film as a mask.

Step 15: In the above step 10, the pixel electrodes were formed after etching the semiconductor layer.

Further features of the present invention to realize the above objects are as follows:

- (1) A semiconductor device comprising an insulating substrate whereon a semiconductor pattern consisting of gate electrodes, insulating layer, and semiconductor layer, and source electrodes and drain electrodes formed so as to cross the gate electrodes in the above semiconductor pattern region are provided, wherein the gate electrodes the end portion of which is tapered, and the semiconductor pattern formed on the gate electrodes the end portion of which is tapered are formed so that the taper angle θ_g of the gate electrodes is made to be equal to or less than three times the taper angle θ_s of the end portion of the semiconductor pattern (where $\theta_g < 90^\circ$).

(2) A semiconductor device as described above, wherein the gate electrodes are composed of a material selected from Ta, Indium-Tin-Oxide (hereinafter called ITO), MoSi_2 , TaSi_2 , CrSi_2 , WSi_2 , TiN, and TaN, and the taper angle θ_g of the gate electrode is made to be equal to or less than two times the taper angle θ_s of the end portion of the semiconductor pattern (where $\theta_g < 90^\circ$).

(3) A semiconductor device as described in the above paragraph (1), wherein the gate electrodes are composed of a material selected from Cr, Mo, W, Al, Cu, Au, and Ni, and the taper angle θ_g of the gate electrode is made to be equal to or less than three times the taper angle θ_s of the end portion of the semiconductor pattern (where $\theta_g < 90^\circ$).

(4) A semiconductor device as described in the above paragraph (1), wherein the taper angle θ_g of the gate electrode is in the range of 0.5-3 times the taper angle θ_s of the end portion of the semiconductor pattern (where $\theta_g < 90^\circ$).

(5) A semiconductor device as described in the above paragraph (1), wherein the taper angle θ_g of the gate electrode is in the range of 10 to 40° .

(6) A semiconductor device as described in the above paragraph (1), wherein the gate electrode the end portion of which is tapered, and the semiconductor pattern, formed on the gate electrode, the end portion of which is tapered are formed, and the gate electrode and the semiconductor pattern are designed such that the ratio (taper ratio B/A) of the back distance from the end of the lower plane to the end of the upper plane of the gate electrode (A) to the film thickness (B) is equal to or less than three times the taper ratio (B'/A') at the end portion of the semiconductor pattern.

(7) A semiconductor device as described in the above paragraph (1), wherein the taper ratio (B/A) of the gate electrode is in the range of 0.2 to 0.8.

(8) A liquid crystal display apparatus comprising thin film transistors which are arranged in the vicinity of respective intersections of a plurality of scanning signal lines and image signal lines which are formed of one of a pair of substrates and of which the gate electrode, the drain electrode and the source electrode are respectively connected to the scanning signal line, the image signal line, and a pixel electrode, wherein the gate electrodes the end portion of which is tapered, and the semiconductor pattern, formed on the gate electrode, the end portion of which is tapered are formed so that the taper angle θ_g of the gate electrode is equal to or less than three times the taper angle θ_s of the end portion of the semiconductor pattern (where $\theta_g < 90^\circ$), and a liquid crystal layer is provided between the substrate and the other, transparent substrate, the substrates being provided with a liquid crystal alignment film.

(9) A semiconductor device as described in the above paragraph (8), wherein the gate electrode the end portion of which is tapered, and the semicon-

ductor pattern, formed on the gate electrode, the end portion of which is tapered are formed, and the gate electrode and the semiconductor pattern are designed such that the ratio (taper ratio B/A) of the back distance from the end of the lower plane to the end of the upper plane of the gate electrode (A) to the film thickness (B) is equal to or less than three times the taper ratio (B'/A') at the end portion of the semiconductor pattern, and a liquid crystal layer is provided between the substrate and the other, transparent substrate, the substrates being provided with a liquid crystal alignment film.

In accordance with the above described features, the length of breakage generated at the tapered end of the semiconductor pattern can be restricted to less than 1/2 of the slope length of the insulating layer. And accordingly, the occurrence of G/D short circuits can be suppressed.

Further, the semiconductor pattern can provide a matrix type liquid crystal display apparatus comprising thin film transistors as an active element which are arranged in the vicinity of the respective intersections of a plurality of scanning signal lines and image signal lines of the liquid crystal display elements, and of which the gate electrodes, the drain electrodes, and the source electrodes are respectively connected in the same layer to the scanning signal line, the image signal line, and a pixel electrode.

The present invention is effective for TFTs having an inverted staggered structure wherein the gate electrode is formed under the semiconductor pattern, and similarly, is effective for TFTs having a normal staggered structure (top gate structure) wherein the source electrode and the drain electrode are formed under the semiconductor pattern.

The semiconductor pattern relating to the present invention can be formed only with the insulating layer or the semiconductor layer, and is designed such that the semiconductor pattern crosses the wiring. Further, the semiconductor pattern can be formed on a wiring board of an ordinary electronic device in a similar manner.

In accordance with the present invention, a simplification of the manufacturing process and an increase in the production yield can be achieved, because, as the opening portions in the gate insulating film are fabricated before forming the metallic film for the source electrodes, and the source electrodes are formed at the opening portions, the end portion of the metallic film does not form an eaves shape against the semiconductor layer even if the semiconductor layer is etched using the metallic film of the source electrode as a mask, and accordingly, breakage of the transparent electrodes can be avoided.

Further, as the gate insulating film under the pixel electrode is provided with an opening portion, the transmissivity can be improved. Furthermore, because the light shielding electrode is formed in the vicinity of the data line, and the opening portion of the data insulating film does not exist above the light shielding electrode, a

high production yield can be obtained, the aperture ratio can be increased, and the brightness of the display image can be improved.

In accordance with controlling the taper angle at the end portion of the electrodes of TFT, which has a structure that the source electrode and the drain electrode override the gate electrode in the semiconductor pattern having the semiconductor layer and the gate insulating layer, to be less than three times the taper angle at the end portion of the semiconductor pattern, preferably in a range of 0.5 to 3 times, the breakage generated at the end portion of the electrodes can be reduced in size, and G/D short circuits can be prevented. Accordingly, a semiconductor device having a high reliability can be obtained.

When the semiconductor pattern is formed by isotropic dry etching, a semiconductor pattern the end portion of which is somewhat tapered, is generally obtained. However, breakage is generated at the tapered end portion, because the etching proceeds faster at the portion overriding the gate electrode than the etching at the plain portion.

If the taper angle at the end portion of the gate electrode is controlled to be less than three times of the taper angle at the end portion of the semiconductor pattern, step coverage of the above insulating layer and the semiconductor layer are improved, a length of the crack generated in the slope at the end portion of the semiconductor pattern can be suppressed in short, leak current from the semiconductor layer caused by failure of insulation at the insulating layer can be suppressed, and short circuit among the gate electrode, the source electrode, and the drain electrode can be prevented.

If the taper angle at the end portion of the semiconductor pattern is larger than 30°, it is not necessary to make the taper angle at the end portion of the gate electrode so small. When the above taper angle at the end portion of the semiconductor pattern is approximately 20°, crack by etching is hardly generated because the insulating layer at the tapered portion becomes thick, and the taper angle at the gate electrode can be less than 60°.

If the taper angle at the end portion of the semiconductor pattern is smaller than 10°, a length of the crack generated in the slope at the insulating layer of the semiconductor pattern can be suppressed in short by making the taper angle at the end portion of the gate electrode less than three times of the above angle, i.e. <30°, and accordingly, G/D short circuit can be prevented.

If the taper angle of the gate electrode is smaller, the length of the crack generated in the slope at the insulating layer of the semiconductor pattern can be smaller, and the effect for reducing the leak current and the effect for preventing the short circuit are increased. However, if the above taper angle is too small to be necessary, a cross sectional area as an electrode decreases, and resistance as the scanning signal line increases. Therefore, the above taper angle is preferably approximately

three times of the taper angle at the end portion of the semiconductor pattern.

The crack generated in the slope at the insulating layer of the semiconductor pattern by etching in the pattern processing is not necessarily prevented perfectly, but if the length of the crack is less than 1/2 of the length of the tapered slope, the probability of generating the above leak current and the short circuit among the gates is small, and electrically stable transistor characteristics can be achieved. If the length of the crack is less than 1/3 of the length of the tapered slope, the stability can be further increased.

In accordance with the present invention, a liquid crystal display apparatus having a large aperture ratio and bright image display can be provided. Further, a low-cost liquid crystal display apparatus and its manufacturing method can be provided because the TFT substrate composing a display panel can be produced by a simple processing including only 5 times photo-resist steps. Furthermore, a liquid crystal display apparatus having a preferable production yield and its manufacturing method can be provided because breakage of lines at the step portion of the transparent conductive film made of ITO can be prevented effectively.

Brief Description of the Drawings

FIG. 1 is a cross-sectional view of the liquid crystal display panel in the embodiment 1 of the present invention (a view taken along the line 1-1 in FIG. 2).

FIG. 2 is a plan view of the patterns of a pixel and layers in its vicinity on a TFT substrate in the embodiment 1.

FIG. 3 is a cross-sectional view of a thin film transistor, the pixel, and the vicinity of a storage capacitor on the TFT substrate in the embodiment 1 of the present invention (a view taken along the line 3-3 in FIG. 2).

FIG. 4 is a plan view showing the vicinity of a connecting portion of a gate terminal GTM and a gate line GL.

FIG. 5 is a cross-sectional view showing the vicinity of a connecting portion of a gate terminal GTM and a gate line GL.

FIG. 6 is a plan view showing the vicinity of a connecting portion of a drain terminal DTM and a data line DL.

FIG. 7 is a cross-sectional view showing the vicinity of a connecting portion of a drain terminal DTM and a data line DL.

FIG. 8 is a plan view for explaining the structure in the periphery of the matrix of the display panel.

FIG. 9 is a flow chart indicating a manufacturing process for the TFT substrate TFTSUB of the liquid crystal display apparatus in the embodiment 1.

FIG. 10 is a cross-sectional view corresponding to the step A in FIG. 9.

FIG. 11 is a cross-sectional view corresponding to the step B in FIG. 9.

FIG. 12 is a cross-sectional view corresponding to the step C in FIG. 9.

FIG. 13 is a cross-sectional view corresponding to the step D in FIG. 9.

FIG. 14 is a cross-sectional view corresponding to the step E in FIG. 9.

FIG. 15 is a cross-sectional view corresponding to the step F in FIG. 9.

FIG. 16 is a cross-sectional view corresponding to the step G in FIG. 9.

FIG. 17 is a cross-sectional view of the thin film transistor and the storage capacitor when a Cr electrode of the data line is manufactured by the manufacturing method of the present invention.

FIG. 18 is a cross-sectional view of the thin film transistor and the storage capacitor when a transparent pixel electrode is formed by the manufacturing method of the present invention.

FIG. 19 is a plan view of the patterns of a pixel and layers in its vicinity on a TFT substrate in the embodiment 2.

FIG. 20 is a cross-sectional view taken along the line 20-20 in FIG. 19.

FIG. 21 is a plan view of the patterns of a pixel and layers in its vicinity on a TFT substrate in the embodiment 3.

FIG. 22 is a cross-sectional view taken along the line 22-22 in FIG. 21.

FIG. 23 is a cross-sectional view taken along the line 1-1 in FIG. 24.

FIG. 24 is a plan view of the patterns of a pixel and layers in its vicinity on a TFT substrate in the embodiment 4.

FIG. 25 is a schematic perspective view of a thin film transistor of the present invention.

FIGs. 26 (a), 26 (b), and 26 (c) are plan views of the thin film transistor of the present invention.

FIG. 27 is a schematic perspective view of a thin film transistor of the prior art.

FIG. 28 is a graph indicating a relationship between concentrations of nitric acid and ceric nitrate ammonium in an etching agent and a taper angle θ_g of the gate electrode.

FIGs. 29 (a), 29 (b), and 29 (c) are schematic cross-sectional views indicating shapes of the taper at the end portion of the line pattern.

FIG. 30 is a graph indicating a relationship between the taper angle θ_g of the gate electrode and withstand voltage between gate/drain electrodes.

FIGs. 31 (a), 31 (b), and 31 (c) are plan views of overriding portion of the gate electrodes.

FIG. 32 is a schematic cross-sectional view of a liquid crystal display apparatus of the present invention.

Detailed Description of the Embodiments

The liquid crystal display apparatus of the present invention and manufacturing methods therefor are

described hereinafter referring to concrete embodiments.

(Embodiment 1)

FIG. 1 is a cross-sectional view showing the structure of the matrix portion (display portion) of display panel in a liquid crystal display apparatus of active matrix type according to the present embodiment. The display panel comprises a TFT substrate TFTSUB made of a transparent glass substrate SUB1 having thin film transistors, pixel electrodes, and various kinds of wiring and others formed on one side surface, a counter substrate OPSUB made of another transparent glass substrate SUB2 having common electrodes ITO2, color filters FIL, and light shielding film BM and others formed on one side surface, and a liquid crystal layer LC filled in the space between the two substrates facing each other.

The electro-optical state of the liquid crystal layer LC between the above substrates is controlled by applying an image signal voltage between the pixel electrode and the common electrode ITO2 to change the light transmitting state in the portion of the display panel and to display a given image.

A back light is placed at the counter substrate OPSUB side or the TFT substrate TFTSUB side outside the liquid crystal panel to observe the light transmitted through the pixel portion of the liquid crystal panel from the counter side to the back light.

In the figures to be described hereinafter, the parts having the same function are identified by the same reference symbols.

(TFT substrate)

FIG. 2 is a plan view showing the patterns in a pixel and the vicinity thereof forming each of the layers of a TFT substrate TFTSUB. FIG. 1 is a cross-sectional view taken along the line 1-1 in FIG. 2, and FIG. 3 is a cross-sectional view taken along the line 3-3 in FIG. 2.

Next, the structure of the TFT substrate TFTSUB is described in detail referring to FIGs. 1-3. As shown in FIG. 2, a plurality of gate lines (scanning signal lines or horizontal signal lines) GL in parallel to one another and a plurality of data lines (image signal lines or vertical signal lines) DL in parallel to one another intersecting with the gate lines are provided at the surface of the TFT substrate. The region surrounded by two adjacent gate lines GL and two adjacent data lines DL becomes a pixel, and a pixel electrode is formed almost all over the region. A thin film transistor (the region surrounded with a dashed line in FIG. 2) as a switching element is formed at the protruding portion on the gate line (in FIG. 2, protruding portion upwards) corresponding to each of the pixel electrodes, and the source electrode SD1 thereof is connected to the pixel electrode. The scanning voltage applied to the gate line GL is transferred to the gate electrode of the TFT composed of a part of the gate line to turn the TFT in the ON state. At this time, the image sig-

nal supplied to the data line DL is input to the pixel electrode through the source electrode SD1.

(Thin film transistor TFT)

As shown in FIG. 3, the gate line GL is formed on the transparent glass substrate SUB1, and a thin film transistor is composed by forming an insulating layer, a semiconductor layer, and others on the gate line as described later. The thin film transistor operates such that the channel resistance between the source and the drain (data line DL) becomes small when a bias voltage is applied to the gate line GL, and the channel resistance becomes large when the bias voltage is turned to zero.

A gate insulating film GI made of silicon nitride is formed on the gate electrode which is composed of a part of the gate line GL, and an i-type semiconductor layer AS made of amorphous silicon which is intentionally not added with impurities and an N-type semiconductor layer made of amorphous silicon which is added with impurities d0 are formed on the gate insulating film. The i-type semiconductor layer AS composes an active layer of the thin film transistor. The thin film transistor is composed by forming further a source electrode SD1, and a drain electrode (in the present embodiment, a part of the data line DL composes the drain electrode, and the drain electrode is called as the data line DL if it is not specially described) on the i-type semiconductor layer.

As for the source electrode SD1, for example, a silicon nitride film formed by plasma CVD is employed such as to have a thickness of 2000-5000 Å (in the present embodiment, approximately 3500 Å).

The i-type semiconductor layer AS is formed such as to have a thickness of 500-2500 Å (in the present embodiment, approximately 2000 Å). The N-type semiconductor layer d0 is provided to form ohmic-contacts of the i-type semiconductor layer AS with the source electrode and the drain electrode, and is made of amorphous silicon semiconductor doped with phosphorus (P).

The names of the source electrode and the drain electrode are determined naturally by the polarity of the bias voltage applied between the above electrodes. In the liquid crystal display apparatus relating to the present invention, the source electrode and the drain electrode are altered mutually because the polarity changes during operation. However, in the following description, for the purpose of simplification it is fixed that one is called as the source electrode and the other is called as the drain electrode.

(Source electrode)

As shown in FIG. 3, the source electrode SD1 is formed on a region from the N-type semiconductor layer d0 of the thin film transistor TFT to the vicinity of the pixel electrode on the glass substrate SUB1, and is composed of a laminated film comprising a first conductive layer d1 and a second conductive layer d2. The first conductive layer d1 is formed of chromium (Cr) so as to have a thick-

ness of 600-1500 Å (in the present embodiment, approximately 1200 Å), and the second conductive film d2 is formed of transparent conductive film ITO1 such as Indium-Tin-Oxide (hereinafter abbreviated as ITO). The first conductive film d1 may be formed of a high melting metal (Ti, Ta, W, Mo) other than Cr, and of alloys of the above metals.

The above source electrode SD1 is formed so as to extend into inside of the opening portion of the gate insulating film GI (in FIG. 3, indicated as the pixel electrode) which is formed inside of a pixel region as shown in FIGS. 2 and 3. That is, as shown in FIG. 3, the first conductive film d1 forming the source electrode SD1 and the second conductive film d2 thereon are formed in the pixel region so that at least a part of them contact with the glass substrate SUB 1.

In accordance with the above structure, the transparent electrode d2 can preferably override the step at the lower first conductive film d1 without causing any breakage of line. The above structure will be described in detail later in connection with the description on manufacturing method. Especially, the above effect is significant when the transparent conductive film d2 is made of ITO as in the present embodiment. Because ITO has a large crystal grain size, the etching speed at the grain boundary part of the crystal grains differs from the etching speed at the crystal grains themselves, and is faster than that at the crystal grains themselves. Therefore, if the step portion under the transparent conductive film d2 is not manufactured in a proper tapered shape, the ITO readily causes breakage of line.

In view of the above aspect, if the semiconductor is etched using the metallic film as a mask on the semiconductor film as disclosed in JP-A-61-161764 (1986), the metallic film is formed in an eaves shape in the cross sectional structure, and the transparent conductive film readily causes breakage of line. On the contrary, the breakage of line at the step portion hardly occurs as described above.

As described later in connection with the manufacturing method, the opening of the gate insulating film GI is formed before forming of the first conductive film d1 in the present embodiment, and the first conductive film d1 is formed on the glass substrate SUB1 exposed by the previous process for forming the opening. When a gas containing fluorine, which is a conventional dry etching gas for the semiconductor, is used for the dry etching, a dry etching speed of the glass is slower than that for the semiconductor silicon. Therefore, the present embodiment has feature such that the end portion of the first conductive film d1 does not form the eaves shape even if the i-type semiconductor AS is selectively etched against the gate insulating film GI using the first conductive film as a mask, the second conductive film composing the source electrode SD1 does not cause any breakage of line, and a preferable production yield can be obtained.

Further, in accordance with forming the opening at the gate insulating film GI, light absorption at the pixel

tangular storage capacitor TCadd has another effect as described hereinafter. That is, as the TCadd is formed at the convex portion of the gate line GL, a static shield effect of the convex portion reduces static effect given to the pixel capacitor (a capacitor formed by the pixel electrode, the transparent conductive film ITO2 formed on the counter substrate, and the liquid crystal layer held between the above electrode and film) by change in voltage of the data line DL.

(Passivation film)

As shown in FIGs. 1 and 3, the surface of the TFT substrate TFTSUB in the side having the thin film transistor is covered with a passivation film PSV1 except the center portion of the pixel electrode, and the gate terminal portion and the drain terminal portion provided in the periphery of the TFT substrate as described later. By forming an opening of the passivation film PSV1 at an upper portion of the pixel electrode, light absorption by the passivation film at the opening portion can be eliminated, and accordingly, transmissivity of the display panel, i.e. brightness, can be increased. The passivation film PSV1 is formed for mainly protecting the thin film transistor TFT from moisture, and others. The passivation film PSV1 is formed of silicon oxide film or silicon nitride film of 2000 Å - 8000 Å thick by, for example, plasma CVD.

(Gate terminal portion GTM)

FIG. 4 is a plan view showing the area from the end portion of the gate line GL on the TFT substrate to a gate terminal GTM which is a connecting portion with an external driving circuit, and FIG. 5 is a cross sectional view taken along the line 5-5 in FIG. 4.

The gate terminal GTM is composed of a laminated films of the conductive film g1 forming the gate line GL, and the first conductive film d1 and the transparent conductive film d2 forming the data line DL. The transparent conductive film d2 is exposed to the external. The transparent electrode formed of ITO protects the first conductive film d1 and the conductive film g1 under the d1 made of Cr from the exterior environment. The transparent conductive film of the gate terminal GTM is formed together with the transparent conductive films ITO1 forming the pixel electrode and the data line. The first conductive film d1 has a larger pattern than that of the conductive film g1, and the transparent conductive film d2 has a larger pattern than the first conductive film d1. The reason is to prevent losing the conductive film g1 formed of chromium as same as the first conductive film d1 after forming the gate insulating film GI, and to prevent corrosion of the conductive film g1 and the first conductive film d1 formed of chromium due to entering of chemicals or moisture. In the above construction, The transparent conductive film ITO1 (d2) is only one exposed portion to the external other than the passivation film PSV1. The ITO is oxides, and is significantly resistant to oxidation reactions which

cause the corrosion. Therefore, the above described structure has a strong reliability.

As described above, the liquid crystal display apparatus using TFT can be manufactured with a preferable production yield and be improved in reliability by coating the metallic conductive film composing the gate terminal GTM with ITO. In the above point of view, the opening of the gate insulating film GI under the transparent conductive film d2 formed of ITO must be manufactured before forming the d2. Further, the i-type semiconductor AS and the gate insulating film GI at the step portions under the ITO must be manufactured in a preferable taper, as previously described.

(Drain terminal GTM)

FIG. 6 is a plan view showing the area from the end portion of the data line DL on the TFT substrate to a connecting portion to an external driving circuit of a drain terminal DTM, and FIG. 7 is a cross sectional view taken along the line 7-7 in FIG. 6.

With the same reason as the above described gate terminal GTM, the drain terminal DTM is composed of two layers of the first conductive film d1 made of chromium composing the data lines DL and the transparent conductive film d2 made of the transparent conductive film. The transparent conductive film is formed with a wider pattern than that of the first conductive film. The passivation film PSV1 in the portion of the drain terminal is removed so as to be connected with to an external circuit.

FIG. 8 is a plan view showing the structure in the peripheral portion of the display panel. In the periphery of the TFT substrate TFTSUB (SUB1), the plural gate terminals GTM corresponding to each of the gate lines are arranged to form a group of gate terminals Tg. Similarly, the plural drain terminals DTM corresponding to each of the data lines are arranged to form a group of drain terminals Td. The INJ in FIG. 8 is a portion whereon the seal pattern SL for adhering the TFT substrate TFTSUB and the counter substrate OPSUB is not formed, and after the above two substrates are adhered, liquid crystal is filled from the portion.

(Counter substrate OPSUB)

As shown in FIG. 1, a shielding film BM, a color filter having three colors of red, green, and blue FIL, a passivation film PSV2, common transparent pixel electrode ITO2, and an alignment film OPRI2 are successively laminated on one side surface of the transparent glass substrate SUB2. A polarizing plate POL2 is adhered to another side surface of the transparent substrate SUB2. Transmitted light is polarized by the above polarizing plate POL2 and the polarizing plate POL1 which is adhered to one side surface of the TFT substrate TFTSUB whereon the TFT is not formed.

The above shielding film BM is formed of chromium spattered film, so that the shielding film performs two

functions, one is a shielding function to shields light from the uncontrolled region of the display panel, and another is a black matrix function to improve contrast by surrounding periphery of each pixel as a picture frame.

(Manufacturing method of the TFT substrate TFTSUB)

Next, the manufacturing method of the above described TFT substrate TFTSUB is described herein-after referring to FIGs. 9-16. FIG. 9 is a flow chart summarizing a flow of manufacturing steps in a manufacturing process using name of each step. A plurality of the steps related each other are gathered for forming a sub-process, and each of the sub-processes is designated by marks as (A), (B), (C), and so on. FIGs. 10-16 correspond to final cross sectional structures at each of the above sub-processes designated as (A) to (G). These figures are cross sectional views of the vicinity of the connecting portion of the thin film transistor with the pixel electrode and the storage capacitor on the TFT substrate (refer to the cross sectional view in FIG. 3). FIG. 3 corresponds to the cross sectional structure after finishing the sub-process (H) in FIG. 9. In each of the sub-processes of (A), (C), (D), (F), and (H) includes a photo-treatment process. The photo-treatment process means a series of works from application of photoresist to development through selective exposure using a photomask in the description of the present invention. As FIG. 9 reveals, the TFT substrate of the present embodiment is manufactured through five times of the photo-treatment processes.

FIG. 17 is a cross sectional structure drawn close to the real shape of the respective thin film just before an etching process of a-Si after finishing the third photo-treatment process in the sub-process (D) in FIG. 9. FIG. 18 is similarly a cross sectional structure close to the real shape of the thin films after ITO spattering in the sub-process (F) in FIG. 9. Hereinafter, each process is described successively.

By preparing a transparent glass substrate SUB1, a chromium film is wholly formed on one of the surfaces of the substrate SUB1 by spattering. After forming a mask having a given pattern on the chromium film by a photo-treatment (first photo-treatment), the chromium film is selectively etched to form a conductive film g1 having the given pattern (the process (A), FIG. 10).

Subsequently, on the conductive film g1 formed on the one surface of the transparent glass substrate SUB1, silicon nitride film GI, i-type amorphous silicon film AS, and N-type amorphous film d0 are successively laminated by a plasma CVD apparatus (the process (B), FIG. 11).

After forming a mask by the photo-treatment (second photo-treatment), a portion for becoming a pixel of the respective three layers of the N-type semiconductor layer d0 (N-type amorphous Si), i-type semiconductor layer AS (i-type amorphous Si), and the gate insulating film GI (silicon nitride) is removed by etching using SF₆ gas (the process (C), FIG. 12).

Next, a chromium film is formed on the above processed substrate by spattering. After forming a mask having a given pattern by the photo-treatment (third photo-treatment) on the chromium film, the chromium film is selectively etched to form a conductive film d1. In this treatment, the end portion of the first conductive film d1 extending from the thin film transistor TFT is formed at the opening formed by the above treatment on the transparent glass substrate SUB1 (the process (D), FIG. 13).

Then, using the mask for the first conductive film d1 formed by the previous process, the N-type semiconductor layer d0 and the i-type semiconductor layer AS are selectively removed by etching using a mixture of SF₆ and BCl₃ (the process (E), FIG. 14).

Next, a transparent conductive film d2 made of ITO film is formed by spattering. After forming a mask by the photo-treatment (fourth photo-treatment), the transparent conductive film is selectively etched using HBr solution to form an ITO pattern on the transparent conductive film ITO1 (the process (F), FIG. 15).

Next, the first conductive film d1 is selectively etched again using the pattern-formed transparent conductive film d2, and further, the source electrode SD1 and the data line DL is separated by etching the N-type amorphous silicon (the process (G), FIG. 16).

Then, a silicon nitride film is formed by a plasma CVD apparatus. After forming a mask by the photo-treatment (fifth photo-treatment), the silicon nitride film is etched to form the passivation film PSV1 at a region except middle portion of the pixel electrode and others (the process (H), FIG. 3).

Feature of the present invention is further described in detail referring to FIGs. 17 and 18. In accordance with the manufacturing method of the present embodiment, the step portion which does not cause wire breakage can be obtained even if using ITO which readily causes wire breakage by the step existing under it.

FIG. 17 is a cross sectional view showing a structure soon after the chromium etching in the third photo-treatment indicated in FIG. 9. The photoresist PRES used as a mask is remained on the first conductive film d1.

The end portions of the N-type semiconductor layer d0, the i-type semiconductor layer AS, and the gate insulating film GI, all of which are the steps under the first conductive film d1, are formed in preferable tapers, respectively. The tapers of these three layers are obtained by a continuous etching using SF₆ gas of which main component is fluorine (F). Ratios of etching speed by SF₆ gas are, taking the speed for the glass substrate SUB1 as 1, approximately 20 for the gate insulating film GI, 80 for the i-type semiconductor layer AS, and approximately 160 for the N-type semiconductor layer d0, such as N-type amorphous Si > i-type amorphous Si > Si nitride film > glass substrate. Accordingly, when etching for the N-type amorphous silicon film is finished and the etching for the i-type amorphous silicon film starts, the upper N-type amorphous silicon is side etched, and consequently, the end portion of the i-type amorphous silicon film is manufactured in a taper (slope) with an angle

of approximately 70-75°. When etching for the i-type amorphous silicon film is finished and the etching for the silicon nitride film starts, the upper N-type amorphous silicon and the i-type amorphous silicon film are consecutively side etched, and consequently, the end portion of the i-type semiconductor layer AS is manufactured in a taper (slope) with an angle of 50°, and the end portion of the gate insulating film GI is shaped in a taper of 20°. Accordingly, a probability of causing wire breakage of the first conductive film d1 formed on them is decreased less than a case existing steep steps without taper. Further, if the tapered portion is coated with the first conductive film d1, the taper angle at the upper surface of the first conductive film d1 formed on the taper becomes approximately 10°.

On the other hand, the end portion of the first conductive film d1 itself on the glass substrate SUB1 becomes approximately 10° by adding an adequate amount of ceric nitrate ammonium and nitric acid to the etching solution.

Next, a case is considered wherein the N-type semiconductor layer d0 and the i-type semiconductor layer AS on the conductive film g1 of the storage capacitor are selectively removed by etching using the photoresist PRES as a mask as shown in FIG. 17. At the etching, a dry etching gas flows as the arrows indicate in FIG. 17, especially, the gas flows round under the end portion of the photoresist PRES at the end portion of the first conductive film d1, and to the glass substrate SUB1 along the taper at the end portion of the first conductive film d1.

A cross sectional view after the transparent conductive film d2 made of ITO is finally coated is shown in FIG. 18. When the N-type semiconductor layer d0 and the i-type semiconductor layer AS on the gate insulating film GI or the glass substrate SUB1 are etched selectively, a mixture of SF₆ gas and BCl₃ gas is used as a dry etching gas. By adding BCl₃ gas, ratios of etching speed become, taken the etching speed for the glass substrate as 1, 5 for the silicon nitride film, 80 for the i-type amorphous silicon film, and 160 for the N-type amorphous silicon film. Therefore, even if the i-type semiconductor layer AS and the N-type amorphous silicon film of the storage capacitor are etched, the silicon nitride film can be remained with a preferable selective ratio. In this process, as the etching speed of the gate insulating film GI is small as 1/4 of the etching speed of the i-type semiconductor layer AS, the gate insulating film is side etched when the i-type amorphous silicon is etched. Consequently, The taper angle TH3 of the silicon nitride film of the storage capacitor decreases to 15°-20° as same as the taper angle TH1 of the silicon nitride film under the first conductive film d1, and becomes preferable for coating the transparent conductive film d2. Further, the etching speed of the glass substrate SUB1 under the first conductive film d1 is remarkably small as previously described, and the taper angle TH 2 is 3°. Furthermore, although it is not shown in the figure, the taper angle of upper surface of the CVD film at the end portion of the conductive film g1 of the storage capacitor is as small as

5°, because the CVD film is preferably coated. The above described advantages can not be lost even if an insulating film having an equivalent dry etching speed against fluorine group gas to the glass substrate such as, for example, a tantalum oxide film is formed on the transparent glass substrate SUB1.

In accordance with the present embodiment, a liquid crystal display apparatus having a high aperture ratio and bright image display can be realized.

Because the TFT substrate composing the display panel can be manufactured by a simple process including only five photoresist treatment, an advantage to provide a cheap liquid crystal display apparatus can be achieved. Further, wire breakage of ITO can be prevented and production yield can be improved because the taper angle at all of the steps under the conductive film made of ITO which readily causes wire breakage can be made equal to or less than 10°.

(Embodiment 2)

The second embodiment of the present invention is explained referring to FIGs. 19 and 20. FIG. 19 is a plan view of a pixel, and FIG. 20 is a cross sectional view taken along the line 20-20 in FIG. 19.

A different point in the present embodiment from embodiment 1 is that, as a structure to improve the aperture ratio, the shielding electrode SKD for a floating electrode is not used, but a rectangular storage capacitor TCadd is enlarged and only the enlarged rectangular storage capacitor is used for shielding. Accordingly, in comparison with the embodiment 1, an effect to shield voltage change of the data line DL by the rectangular storage capacitor TCadd which is a part of the gate line GL becomes large. Therefore, generation of tailing of images vertically in the image display, so called generation of shading, can be suppressed.

However, in this case, a value of the storage capacitance, which is determined by an area of intercrossing region of the gate line GL and the pixel electrode, increases, and a delay time of scanning voltage applied to the gate line GL increases. Therefore, in order to overcome the above increase of the delay time, the conductive film g1 of the gate line GL is made of low resistant wiring material of which main component is aluminum instead of chromium in embodiment 1 as shown in FIG. 20. In order to prevent decreasing the withstand voltage of the gate insulating film by effects of blocking and others, main surface of the aluminum is anodized to form anodized oxide film AO. As described above, by using low resistant aluminum, images having preferable quality can be displayed without increasing delay time of the scanning voltage even if the storage capacitance increases.

Further, as preferable tapers at the step portions under the transparent conductive film ITO1 can be obtained as same as the embodiment 1, wire breakage of the transparent conductive film can be prevented, and the production yield is improved.

(Embodiment 3)

The third embodiment of the present invention is described hereinafter referring to FIGs. 21 and 22. FIG. 21 is a plan view of a pixel, and FIG. 22 is a cross sectional view taken along the line 22-22 in FIG. 21. The cross sectional view taken along the line 3-3 in FIG. 21 is the same as FIG. 1 of the embodiment 1.

A different point in the present embodiment from the embodiments 1 and 2 is that a storage capacitor line HL is newly formed in parallel to the gate line GL, and a storage capacitor Cadd is formed at an intercrossing region of the storage capacitor line HL and the pixel electrode. Accordingly, in comparison with the embodiments 1 and 2, the capacitance which is a load to the gate line GL can be decreased. Therefore, as the delay time of the scanning voltage applied to the gate line GL can be decreased, the same advantage as the embodiment 1 such that a large size display is possible even if chromium film is used as for the conductive film g1 of the gate line GL can be retained.

As shown in FIG. 22, the storage capacitor line HL is formed of the conductive film g1 as same as the gate line GL. The gate insulating film GI under the pixel electrode has two openings holding the storage capacitor line HL between. The end portion of the gate insulating film GI on the storage capacitor line HL has a preferable taper as well as the embodiment 1, and no wire breakage of the transparent electrode ITO1 can be expected.

(Embodiment 4)

The fourth embodiment of the present invention is described hereinafter referring to FIGs. 23 and 24. FIG. 24 is a plan view of a pixel, and FIG. 23 is a cross sectional view taken along the line 1-1 in FIG. 24.

A different point of the present embodiment from the other embodiment is that, as shown in FIG. 23, the shielding electrode SKD made of the gate line material g1 shields all of the portion under the data line DL, and extends to under the pixel electrode ITO1. Accordingly, in an extreme case, a black matrix BM to be provided at the color filter substrate OPTSUB becomes unnecessary. Therefore, in the present embodiment, the aperture ration can be increased, and consuming power of the liquid crystal display can be decreased. If the same consuming power as the other embodiment is used, the brightest liquid crystal display apparatus can be realized. As shown in FIG. 24, the shielding electrode SKD is made of the gate line material g1. However, the gate line GL itself is not formed, and the shielding electrode forms a floating electrode which is not controlled by the gate line GL and the data line DL. Therefore, a large scale liquid crystal display apparatus can be realized without increasing the capacitances of the above lines.

(Embodiment 5)

FIG. 25 is a perspective view of a thin film transistor (TFT) formed on a glass substrate. A chromium film of 100 nm thick is formed on a substrate 1 by a sputtering method. The film is manufactured to form scanning signal lines and gate electrodes 2 by a photoetching process. Subsequently, end portions of the gate electrode are manufactured to form tapers having a taper angle of θ_g by wet etching process.

A silicon nitride film, a non-doped amorphous silicon film, and a phosphine-doped amorphous silicon film are continuously formed and laminated as for respectively a gate insulating layer 4, a semiconductor layer 5, and a contact layer 6 by a plasma chemical vapor deposition method (plasma CVD). Then, the above described laminated films are manufactured for patterns. In order to minimize the number of masks and steps, the patterns are manufactured simultaneously with a same mask by dry etching process. As the dry etching process has an isotropic etching characteristics, side etching proceeds at surface of the laminated film to form a taper having a taper angle of θ_s as shown in FIG. 25.

As for image signal lines, pixel electrodes, source and drain electrodes, an ITO film of approximately 300 nm thick is formed by sputtering method, and pattern manufacturing is performed by wet etching process using photoresist. Channel regions are formed by dry etching of the contact layer 6 using the same photoresist. Finally, a silicon nitride film is formed as for a passivation layer by plasma CVD method.

FIGs. 26(a), 26(b), 26(c) are plan views of overriding portion of the gate electrode 2 of the semiconductor pattern when the taper angle θ_s of the gate insulating layer 4 is set at a constant, approximately 10° (taper ratio = 0.18), and the taper angle θ_g at the end portion of the chromium film, i.e. the gate electrode 2, varies.

In a case when the taper angle θ_g of the gate electrode 2 is in a range of $6^\circ - 10^\circ$ (taper ratio = 0.1-0.18), no crack was observed at the overriding portion of the silicon nitride film. Accordingly, it can be concluded that no crack is generated when the θ_g is as low as equal to or less than 10° .

In a case when the θ_g is approximately three times of the θ_s , that is, in a range of $23^\circ - 25^\circ$ (taper ratio = 0.47-0.7), a crack (C) equivalent to approximately 1/4 of the length at the slope of the taper was generated. However, the electric characteristics of the TFT was not influenced at all by existing such a crack as above described degree at the slope of the taper of the gate insulating layer 4.

However, in a case when the θ_g becomes more than four times of the θ_s , that is, in a range of $70^\circ - 80^\circ$ (taper ratio = 2.7-5.6), a crack (C) more than 1/2 of the length at the slope of the taper was generated. FIG. 27 is a perspective view of the TFT at the above described case. Leak current of the gate electrode 2 and the semiconductor layer 5 increase, and short circuit between the

gate electrode 2 and the drain electrode 8 occur frequently when the crack (C) is large.

The θ_s can be formed in a range of approximately 10° - 30° by dry etching process using SF_6 gas.

Further, θ_g can be controlled by changing composition of an etchant for the chromium film, i.e. the gate electrode 2. The etchant is a mixture including nitric acid, ceric nitrate ammonium, perchloric acid, and water. Among the above components, concentration of ceric nitrate ammonium determines etching speed mainly in a vertical direction. Nitric acid enters into a contacting boundary between the chromium film and the photoresist, and lateral etching proceeds by entering ceric nitrate ammonium into the boundary subsequently to nitric acid. A ratio of the above vertical and lateral etching speed is a key factor for determining the taper angle θ_g at the end portion of the chromium film as the gate electrode 2.

In FIG. 28, ratios of nitric acid and ceric nitrate ammonium for forming the taper angle θ_g of the gate electrode 2 equal to or less than three times of the taper angle θ_s of the gate insulating layer 4 when the θ_s is set as 10° .

A case when concentration of ceric nitrate ammonium is 20 % and nitric acid concentration is 9 mol/l, θ_g becomes 6° - 10° , and if concentration is 8 mol/l, forming the taper becomes impossible.

On the contrary, when concentration of ceric nitrate ammonium is 15 %, the etching speed in a vertical direction becomes smaller than the speed at 20 %. Consequently, the etching speed in a lateral direction increases relatively, and θ_g becomes small. That means, 2° - 3° is obtained at nitric acid concentration of 9 mol/l, and 7° is obtained at 8 mol/l.

Further, θ_g varies depending on adhesiveness of the chromium film and the etching resist in addition to the composition of the etchant. One of the factors to determine the adhesiveness is roughness (RMS) at surface of the chromium film.

In FIG. 28, a relationship between the surface roughness (RMS) of the chromium film and the θ_g is shown. For a film having small RMS such as 1.07 (having small convex and concave at the surface), the θ_g is 10° (when nitric acid concentration is 9 mol/l). On the contrary, even with the same etchant, for a film having RMS of 1.20 (having large convex and concave at the surface), the θ_g becomes 20° , and for a film having RMS of 1.43 (having further large convex and concave at the surface), the θ_g becomes 25° . Therefore, the surface roughness (RMS) of the film can be regarded as an important factor for taper etching of the gate electrode.

Various shapes at the end portion of the pattern are formed by manufacturing the taper such as the one shown in FIG. 29 (a) wherein the slope of the taper can be approximated by a straight line, and the others shown in (b) and (c) which are hardly approximated by a straight line. The taper angle of the case (a) is easily defined, but the cases (b) and (c) are difficult to define the taper angles. In these cases, the taper angle is defined by the ratio of the width of the taper portion, i.e. a recessive dis-

tance from the lower end to the upper end (bottom length: A) and the film thickness (B), so-called a taper ratio (B/A). Accordingly, both the taper ratios (B/A) of the (b) and (c) are defined as same 0.62.

FIG. 30 is a graph indicating a relationship between the taper angle θ_g of the gate electrode 2 and withstand voltage G/D. Cutting lengths of the crack (C) in the gate insulating layer 4 at the overriding portion of the gate electrode 2 are shown at respective measuring points.

When the taper angle θ_s of silicon nitride film, i.e. the gate insulating layer 4, is set as 10° , the withstand voltage G/D has a high value such as 400 V when θ_g is 10° . At the above case, the cutting length of the crack (C) was zero. If θ_g is 30° , a crack (C) of approximately $1 \mu\text{m}$ long is generated, but the crack does not influence to the withstand voltage G/D. However, if θ_g exceeds 30° , the withstand voltage decreases rapidly. The decrease is caused by extending the cutting length of the crack (C) in the gate insulating layer beyond 1/2 of the slope length of the taper.

As for other effects of forming the taper at the end portion of the gate electrode 2 than the above description, wire breakage can be prevented. As shown in FIG. 31, when a material having weak step coverage for the film such as poly ITO film is used for the drain electrode 8, the crack generated by etching enters into the drain electrode 8, and wire breakage of the electrode 8 can be caused (hereinafter, called D-breakage). The d-breakage can be suppressed by setting the taper angle of the gate electrode 2 as 10° - 40° (or the taper ratio as 0.2-0.8).

The θ_g equal to or less than 30° can be formed by using a chromium film etchant, wherein 4-7 parts by weight of nitric acid is mixed with 1 part by weight of ceric nitrate ammonium, for etching the gate electrode 2. Especially, a case when 5 parts by weight of nitric acid is added, θ_g of approximately 10° can be obtained. However, formation of a desired taper angle is difficult with nitric acid of less than 4 parts by weight, because the θ_g becomes too large to the θ_s , and crack is generated in the gate insulating layer 4. If the nitric acid content exceeds 7 parts by weight, the θ_g becomes too small depending on the adhesive condition of the chromium film and the photoresist, and preciseness of the pattern formation of the gate electrode 2 decreases.

If the present embodiment is applied to the manufacturing process for the shielding electrode SKD in FIG. 23, wire breakage of ITO1 can be decreased.

(Embodiment 6)

When conductive material having relatively a large specific resistance (Ta, ITO, MoSi_2 , TaSi_2 , CrSi_2 , WSi_2 , TiN, TaN) is used for manufacturing the gate electrode 2, it is necessary to make its resistance small by increasing its thickness in order to decrease gate delay of the electrode. However, if the thickness increases, the step at the end portion of the gate electrode 2 becomes large, and consequently, cracks are readily generated at the

overriding portion of the gate insulating layer 4 on the gate electrode 2.

In order to make the resistance approximately equal to the one when chromium film of 100 nm thick is used for the gate electrode 2, for instance, forming film thickness of 105 nm for Ta, 1160 nm for poly ITO, 190-775 nm for silicides such as MoSi₂, TaSi₂, WSi₂, and TiSi₂, and 500 nm for TiN and TaN are necessary.

The generation of the crack (C) and G/D short circuit caused by the large step at the end portion of the gate electrode 2 made of the above material could be suppressed by making the θ_g (or taper ratio) of the gate electrode 2 equal to or less than two times of the θ_s (or taper ratio) of the gate insulating layer 4.

On the other hand, when conductive material having relatively a low resistance, for example, such as Al, Cu, Au, Ni, Mo, and W is used for manufacturing the gate electrode 2, the thickness of the electrode must be thin. It is possible to make the electrode with film thickness of 20 nm for Al, 13 nm for Cu, 53 nm for Ni, 44 nm for Mo, and 43 nm for W. In the above case, the generation of the crack (C) and G/D short circuit could be suppressed by making the θ_g (or taper ratio) of the gate electrode 2 equal to or less than three times of the θ_s (or taper ratio) of the gate insulating layer 4.

(Embodiment 7)

When SiO₂ film having a low dielectric constant, or a film made of two layers of SiO₂ and SiN, is used for manufacturing the gate insulating layer 4, it is necessary to make thickness of the film thin as much as the amount equivalent to difference of the dielectric constant in order to obtain the same capacitance as the one in a case when the insulating layer is made of a single layer of SiN.

For example, in order to obtain the same capacitance with a SiN film having a dielectric constant of 2.0 and a film thickness of 350 nm, it is necessary to form a film of 200 nm thick when SiO₂ is used. In the above case, the crack (C) is readily generated at the overriding portion of the SiO₂ gate insulating layer 4 on the gate electrode 2, and generating ratio of electric failure increases.

In the above case, the generation of the crack (C) and G/D short circuit could be suppressed by making the θ_g of the gate electrode 2 as 10° (or taper ratio: 0.17) substantially equal to 10° of the θ_s (or taper ratio: 0.17) of the gate insulating layer 4.

(Embodiment 8)

FIG. 32 is a schematic cross sectional view of a liquid crystal display apparatus using the TFT of the present invention. The liquid crystal display apparatus of TFT drive type was manufactured by the steps of preparing liquid crystal substrate 10 having the TFT formed by the above embodiment of the present invention and a counter substrate 9, arranging alignment films 11 at facing surfaces of both the above substrates 10, 9, and

enclosing liquid crystal 12 between the above alignment films. With the liquid crystal display apparatus, G/D short circuit, leak current, and wire breakage of the ITO drain electrode at the overriding portion of the semiconductor pattern and the drain electrode 8 on the gate electrode 2 can be prevented, and the liquid crystal display apparatus (TFT-LCD) having preferable reliability can be manufactured with a preferable production yield.

Claims

1. Liquid crystal display apparatus, comprising:
a plurality of gate lines (GL) formed on any one of a substrate (SUB1) and an insulating film formed on the substrate,
a plurality of data lines (DL) formed so as to cross the gate lines (GL),
thin film transistors (TFTs) formed in the vicinity of the respective intersections of the gate lines (GL) with the data lines (DL), and
pixel electrodes connected to the thin film transistors (TFTs), and
having the function to drive the liquid crystal, wherein
the central portion of the pixel electrodes is in contact with the substrate (SUB1) or the insulating film formed on the substrate, and
the peripheral portion of the pixel electrode is in contact with an insulating film which was the same layer as the gate insulating film of the thin film transistor (TFT).
2. Apparatus according to claim 1, wherein
a conductive film (ITO1) forming the pixel electrode extends to the source electrode (SD1) of the thin film transistor (TFT), and
the contours in the plain pattern of the conductive film forming the source electrode cross over the contours in the plain pattern at a region of the central portion of the pixel electrode being in contact with the substrate.
3. Apparatus according to claim 1, wherein
a shielding film (SKD,g1) which is in parallel to the data lines (DL) and is separated and insulated from the data lines (DL) by an insulating (GI) film which is the same layer as the gate insulating film (GI) of the thin film transistor (TFT), is provided between the data line (DL) and a region being in contact with the substrate at the central portion of the pixel electrode.
4. Apparatus according to claim 1 or 2, wherein,
a shielding film (SKD,g1) is provided, which shields the lower portion of the data line (DL), extends to the lower portion of the pixel electrode, is separated and insulated from the data lines (DL) and the pixel electrodes by an insulating film which is the same layer as the gate insulating film (GI) of the thin film tran-

- sistor, and is not voltage-controlled by the gate lines (GL).
5. Liquid crystal display apparatus, comprising:
a plurality of gate lines (GL) formed on any one of a substrate (SUB1) and an insulating film formed on the substrate,
a plurality of data lines (DL) formed so as to cross the gate lines (GL),
thin film transistors (TFT) formed in the vicinity of the respective intersections of the gate lines (GL) with the data lines (DL) and
pixel electrodes connected to the thin film transistors (TFTs), and
having the function to drive the liquid crystal, wherein
a shielding film is provided, which shields the lower portion of the data line (DL), extends to the lower portion of the pixel electrode, is separated and insulated from the data lines (DL) and the pixel electrodes by an insulating film which is the same layer as the gate insulating film (GI) of the thin film transistor or by laminated insulating films where one of the films is the gate insulating film (GI), and is not voltage-controlled by the gate lines (GL).
 6. Apparatus according to claim 1, wherein,
a plurality of conductive lines, which correspond to respective of a plurality of the gate lines (GL) and are in parallel to the gate lines (GL), are provided, and capacitor elements are formed by the insulating film between the conductive line and the pixel electrode.
 7. Liquid crystal display apparatus, comprising:
a plurality of gate lines (GL) formed on a substrate (SUB1),
a plurality of data lines (DL) formed so as to cross the gate lines (GL),
thin film transistors (TFT) formed in the vicinity of the respective intersections of the gate lines (GL) and the data lines (DL),
pixel electrodes connected to the thin film transistors (TFTs), and
storage capacitors (Cadd) connected to the pixel electrodes having the function to drive the liquid crystal, wherein
the thin film transistor (TFT) has a structure comprising
a gate insulating film (GI) formed on a gate electrode formed from a part of the gate line (GL),
a semiconductor layer formed on the gate insulating film (GI), and
a source electrode (SD1) and a drain electrode (DL) formed on the semiconductor layer,
the conductive film comprised in the pixel electrode extends on the source electrode (SD1), and
the storage capacitor (Cadd) has a structure comprising an insulating film which is the same layer as the gate insulating film (GI) formed on the gate line (GL) adjacent to the gate line whereon the thin film transistor is formed, and
a conductive film extending from the pixel electrode formed on the insulating film.
 8. Apparatus according to claim 7, wherein
the taper angle formed by the end portions of the gate insulating film (GI) and the semiconductor with the substrate is larger than the taper angle formed by the end portion of the insulating film comprised in the storage capacitor (Cadd) with the substrate.
 9. Apparatus according to claim 7 or 8, wherein
the source electrode (SD1) is in contact with the semiconductor layer, the gate insulating film (GI), and the substrate (SUB1).
 10. Apparatus according to one of claims 7 to 9, wherein
the plurality of the data lines (DL) comprises the semiconductor layer and
a conductive film forming the source electrode (SD1) and the drain electrode, and
the semiconductor layer and the conductive film have the same plane pattern.
 11. Apparatus according to any of claims 7 to 10, wherein the gate line (GL) is coated with an anodic oxide film of the conductive film forming the gate line (GL).
 12. Manufacturing method for liquid crystal display apparatus comprising
a plurality of gate lines (GL) formed on a substrate (SUB1),
a plurality of data lines (DL) formed so as to cross the gate lines (GL),
thin film transistors (TFTs) formed in the vicinity of the respective intersections of the gate lines (GL) with the data lines (DL), and
pixel electrodes connected to the thin film transistors (TFTs), and
having the function to drive the liquid crystal, particularly for manufacturing the liquid crystal display apparatus according to claims 1 to 11, comprising the steps of
etching both the gate insulating film (GI) and the semiconductor layer formed on the gate insulating film (GI) in the same process with approximately the same plain pattern, and subsequently
selectively etching the semiconductor layer.
 13. Method according to claim 12, wherein
a metallic film of a given pattern is formed on the semiconductor layer after etching the gate insulating film and the semiconductor layer in the same process, and subsequently,
the semiconductor layer is etched using the metallic film as a mask.

14. Method according to claim 11 or 12, wherein a step of anodizing the surface of the gate lines is further provided.
15. Method according to claims 11 to 14, wherein sulfur hexafluoride is used as an etching gas in the process of etching the gate insulating film and the semiconductor layer in the same process.
16. Method according to claims 11 to 14, wherein a mixed gas of sulfur hexafluoride and chlorine is used as an etching gas in the process of etching the semiconductor layer using the metallic film as a mask.
17. Method according to claims 11 to 16, wherein the pixel electrodes are formed after etching the semiconductor layer.
18. Semiconductor device provided with a semiconductor pattern comprising a gate electrode (GL), an insulating layer, and a semiconductor layer on an insulating substrate, and a source electrode (SD1) and a drain electrode (DL) which are formed so as to cross over the gate electrode (GL) in the semiconductor pattern region, wherein the semiconductor pattern, the end portion of which is tapered, is formed on the gate electrode, the end portion of which is tapered, and the taper angle θ_g of the gate electrode is made so as to be equal to or less than three times the taper angle θ_s (where θ_g is less than 90°) at the end portion of the semiconductor pattern.
19. Semiconductor device according to claim 18, wherein the gate electrode (GL) is made of a material selected from Ta, ITO, MoSi_2 , TaSi_2 , CrSi_2 , WSi_{21} , TiN, and TaN.
20. Semiconductor device according to claim 18, wherein the gate electrode is made of a material selected from Cr, Mo, W, Al, Cu, Au, and Ni.
21. Semiconductor device according to any of claims 18 to 20, wherein the taper angle θ_g of the gate electrode is in the range of 0.5-3 times (where θ_g is less than 90°) the taper angle θ_s at the end portion of the semiconductor pattern.
22. Semiconductor device according to any of claims 18 to 20, wherein the taper angle θ_g of the gate electrode is in the range of 10 to 40° .
23. Semiconductor device provided with a semiconductor pattern comprising a gate electrode (GL), an insulating layer, and a semiconductor layer on an insulating substrate, and a source electrode (SD1) and a drain electrode (DL) which are formed so as to cross over the gate electrode (GL) in the semiconductor pattern region, wherein the semiconductor pattern, the end portion of which is tapered, is formed on the gate electrode, the end portion of which is tapered, and the gate electrode and the semiconductor pattern are designed such that the ratio (taper ratio B/A) of the back distance from the end of the lower plane to the end of the upper plane of the gate electrode (A) to the gate electrode thickness (B) is equal to or less than three times the taper ratio (B'/A) at the end portion of the semiconductor pattern.
24. Semiconductor device according to claim 23, wherein the taper ratio (B/A) of the gate electrode is in the range of 0.2 to 0.8.
25. Liquid crystal display apparatus, comprising thin film transistors (TFT), which are arranged in the vicinity of respective intersections of a plurality of scanning signal lines with a plurality of image signal lines, both of which are formed on one substrate of a pair of substrates so as to cross over each other, and of which the gate electrodes, the drain electrodes, and the source electrodes are respectively connected to the scanning signal lines, the image signal line, and the pixel electrodes, wherein the semiconductor pattern the end portions of which is tapered is formed on the gate electrode the end portion of which is tapered, the taper angle θ_g of the gate electrode is made to be equal to or less than three times the taper angle θ_s of the end portion of the semiconductor pattern (where θ_g is less than 90°), and a liquid crystal layer is comprised between the substrate and the other, transparent substrate, the substrates being provided with a liquid crystal alignment film.
26. Liquid crystal display apparatus, comprising thin film transistors (TFT), which are arranged in the vicinity of respective intersections of a plurality of scanning signal lines with a plurality of image signal lines, both of which are formed on one substrate of a pair of substrates so as to cross over each other, and of which the gate electrodes, the drain electrodes, and the source electrodes are respectively connected to the scanning signal lines, the image signal line, and the pixel electrodes, wherein the semiconductor pattern the end portion of which is tapered is formed on the gate electrode the end portion of which is tapered, the gate electrode and the semiconductor pattern are so composed that the ratio (taper ratio B/A) of the back distance from the end of the lower plane to the end of the upper plane of the gate electrode (A) to the film thickness (B) of the gate electrode is equal

to or less than three times the taper ratio (B/A') at the end portion of the semiconductor pattern, and a liquid crystal layer is comprised between the substrate and the other, transparent substrate, the substrates being provided with a liquid crystal alignment film.

10

15

20

25

30

35

40

45

50

55

FIG. 1

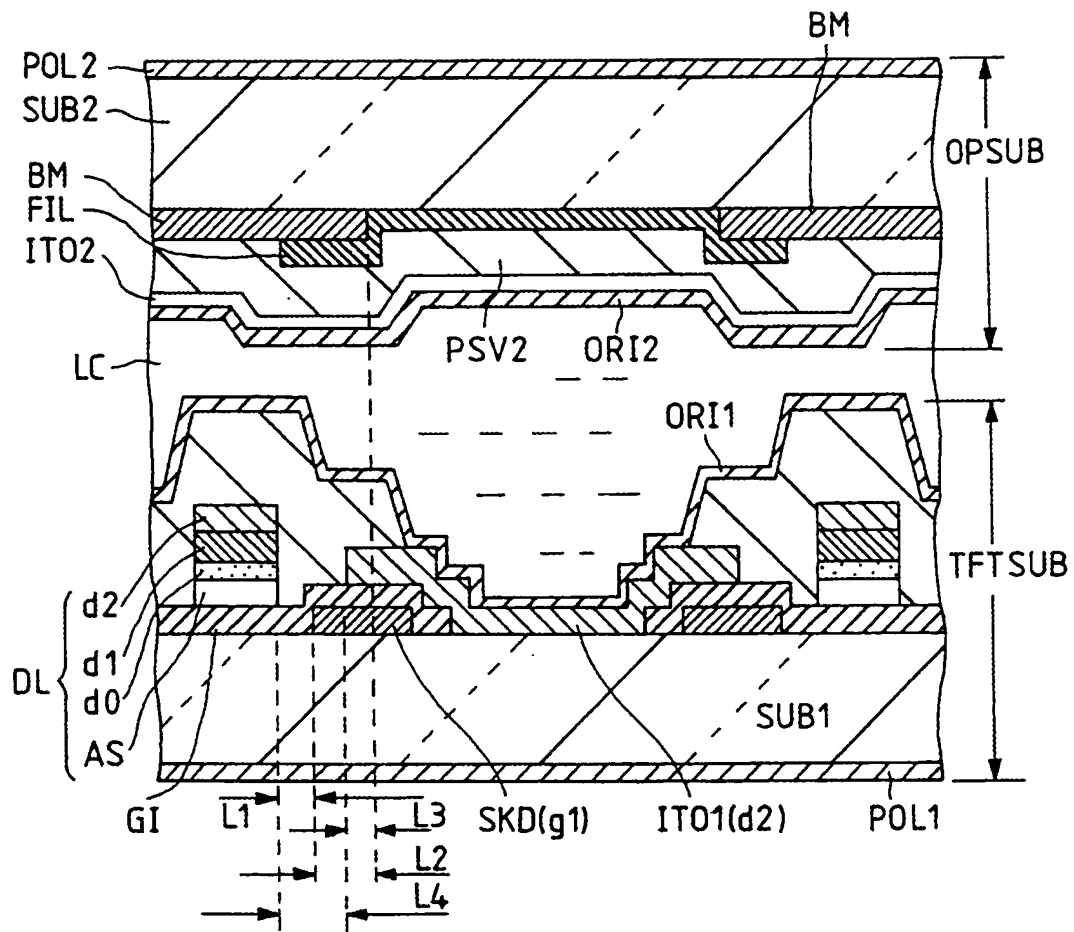


FIG. 2

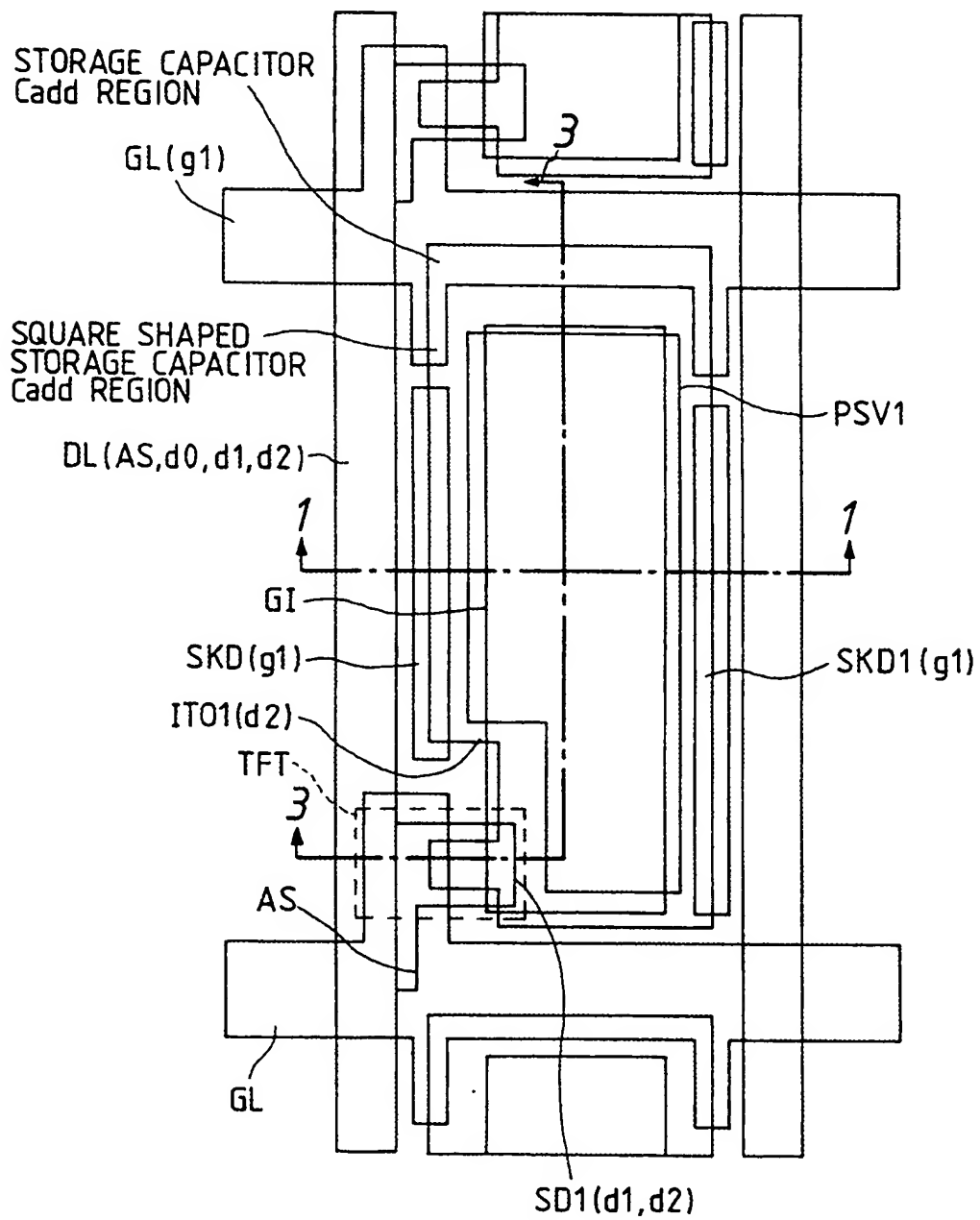


FIG. 3

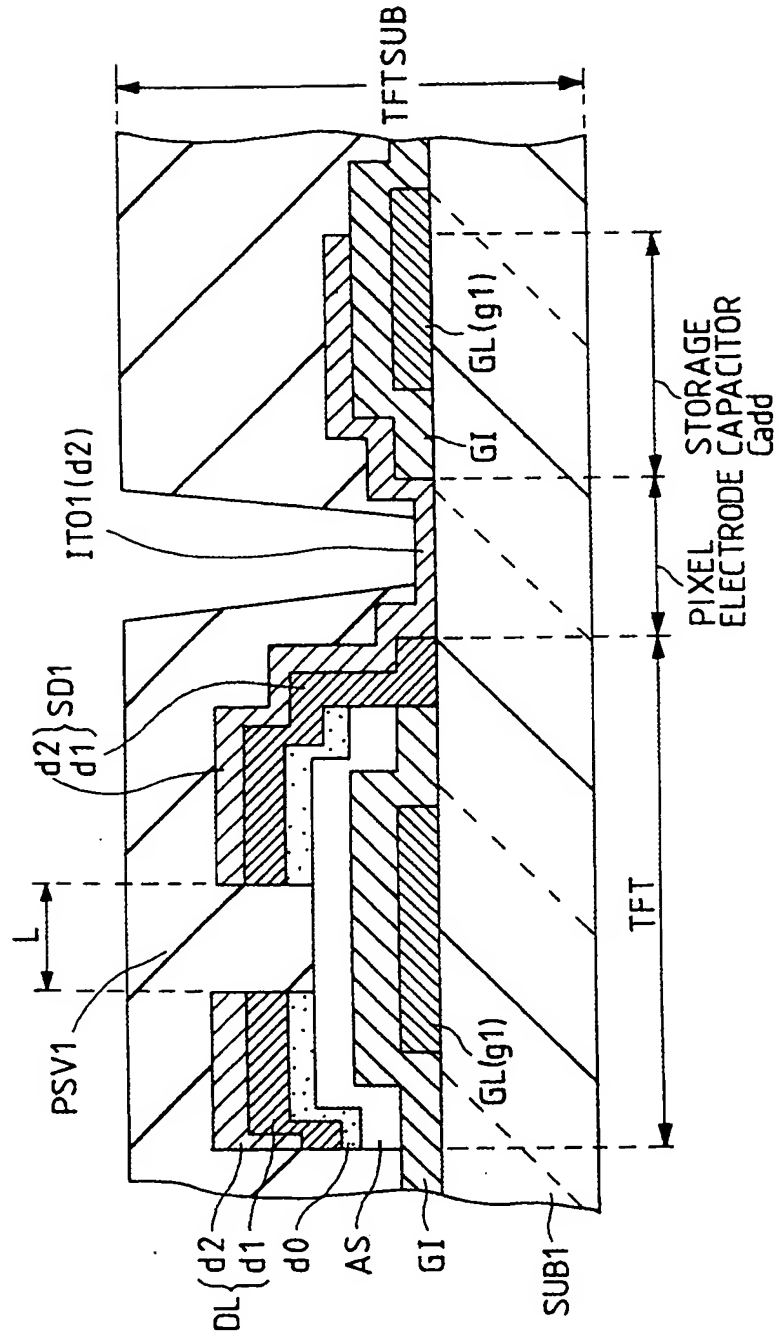


FIG. 4

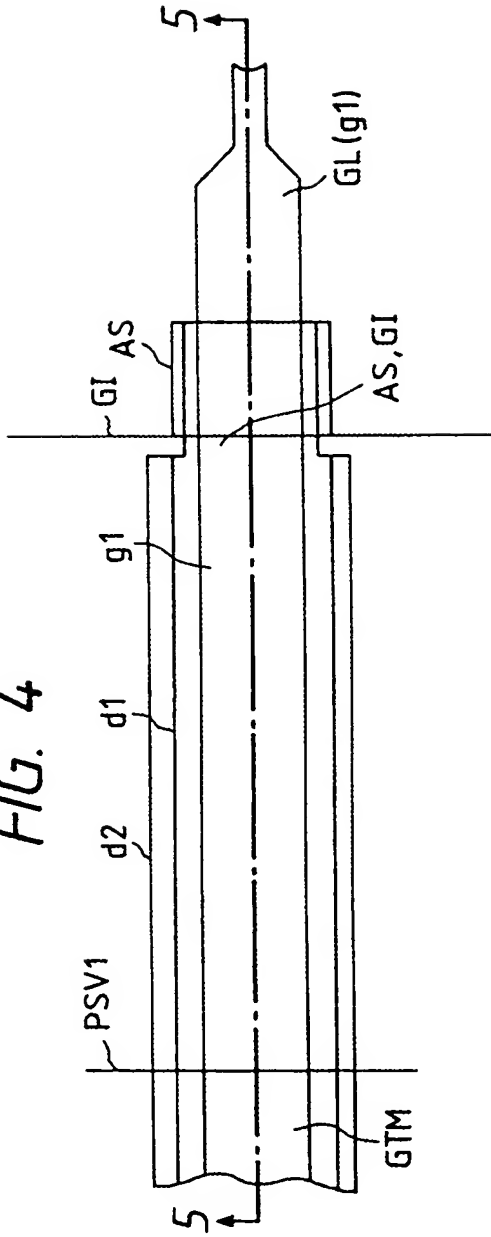


FIG. 5

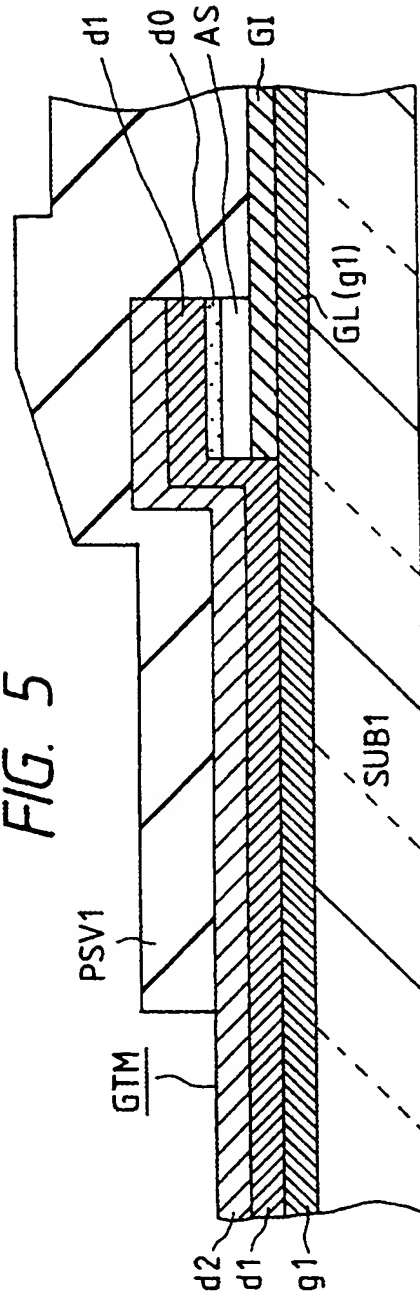


FIG. 6

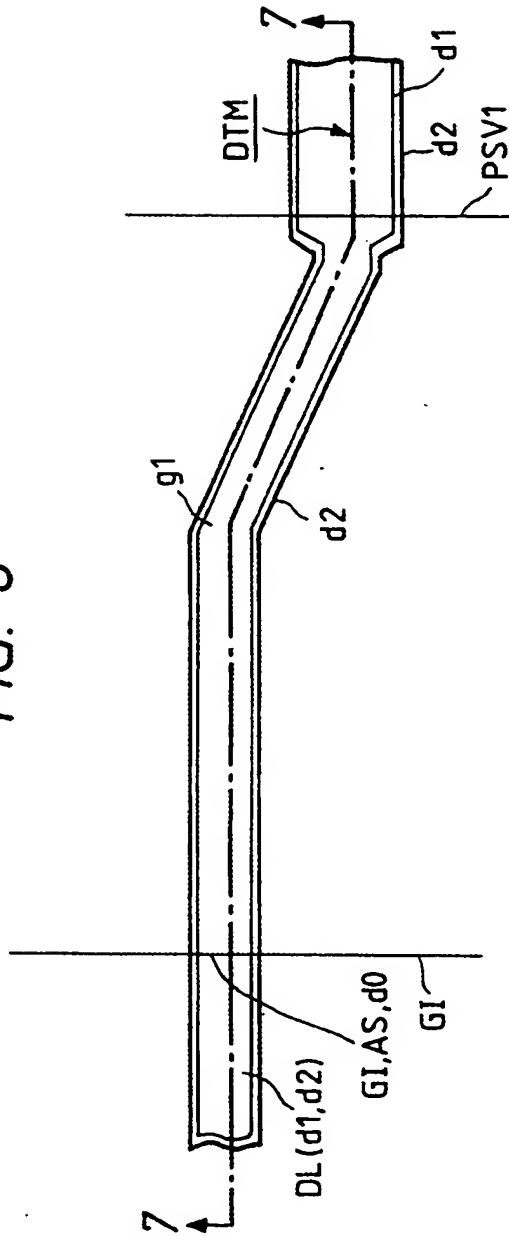


FIG. 7

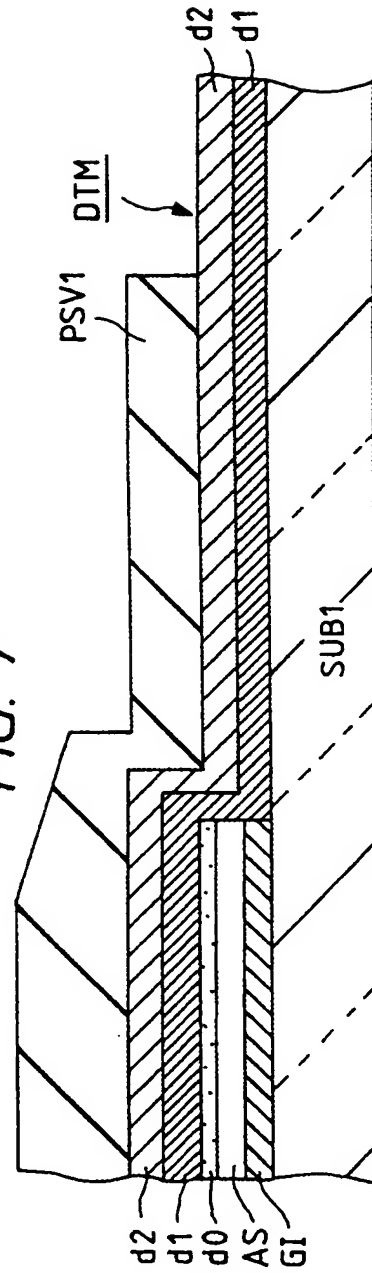


FIG. 8

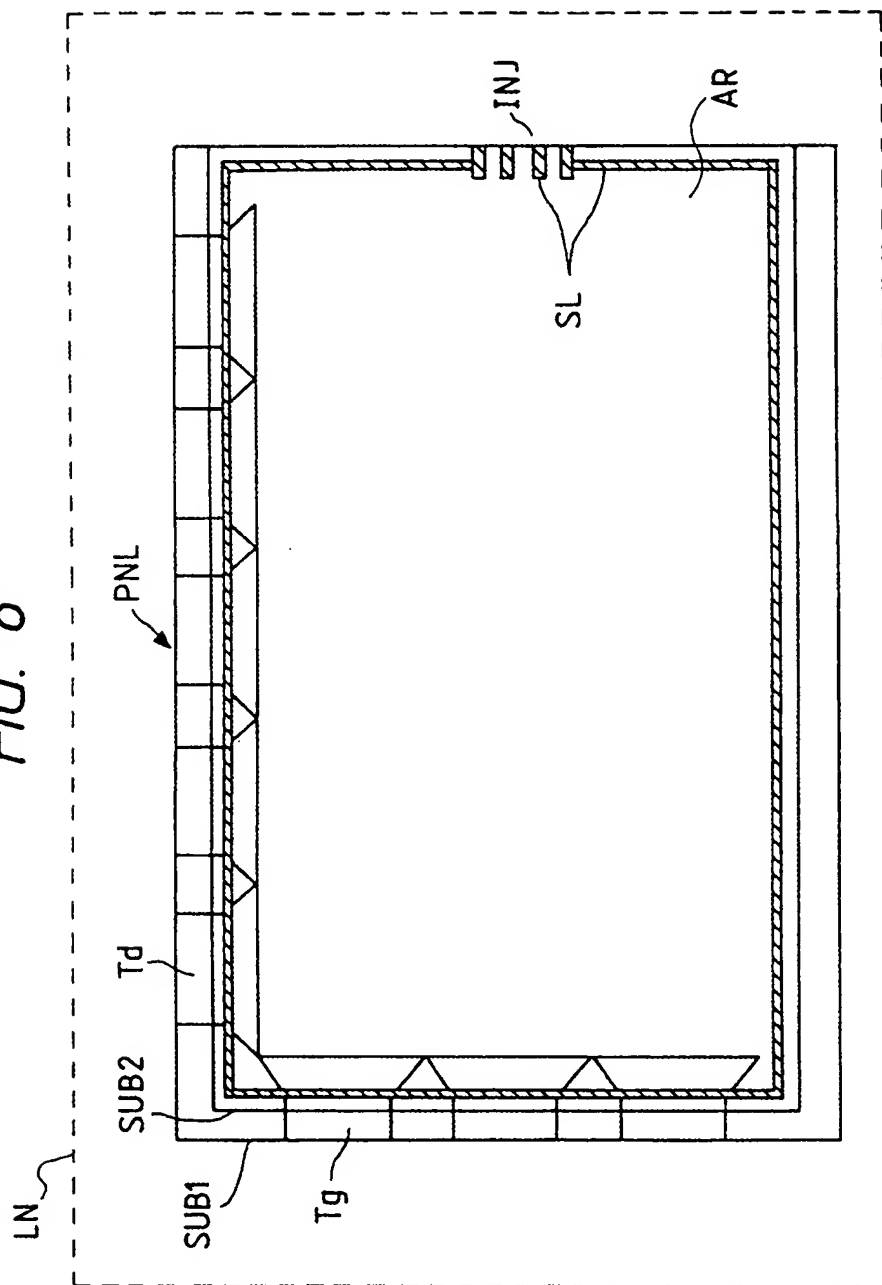


FIG. 9

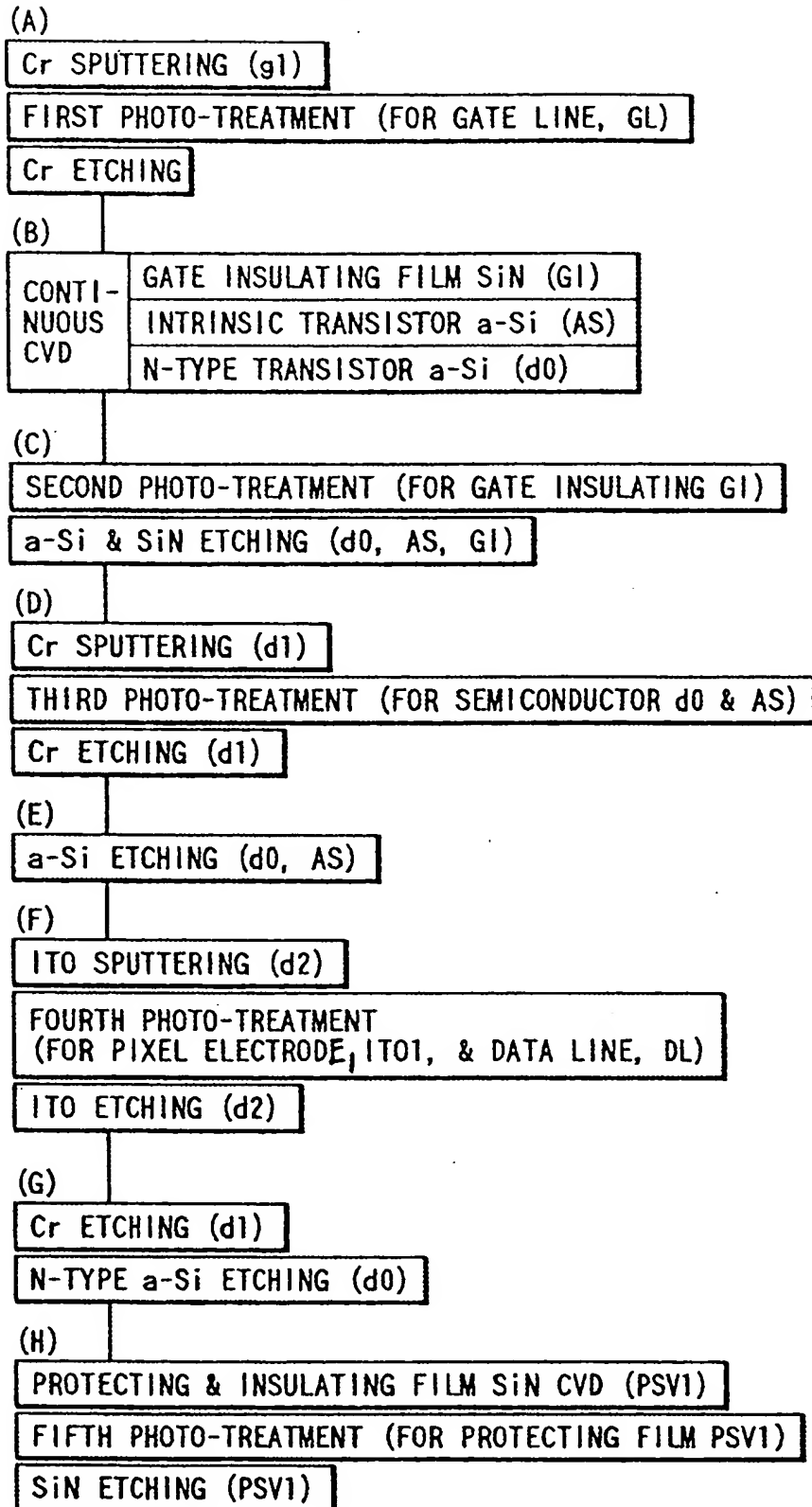


FIG. 10

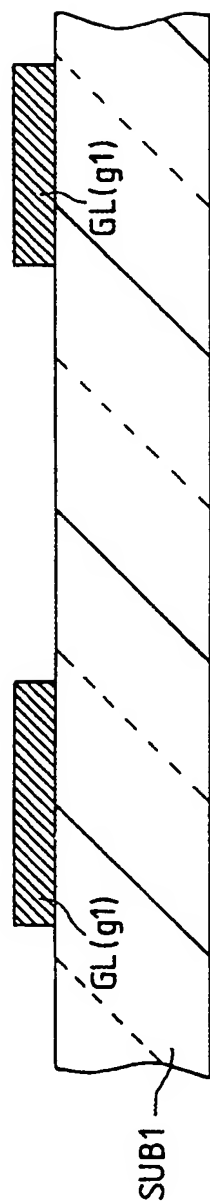


FIG. 11

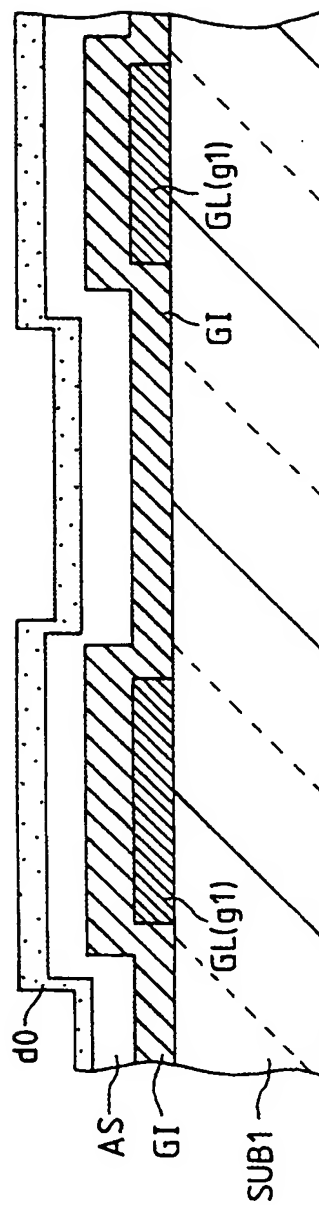


FIG. 12

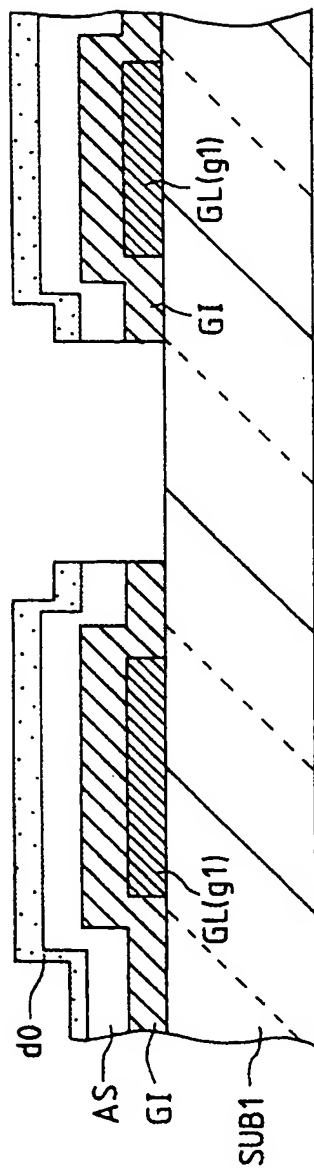


FIG. 13

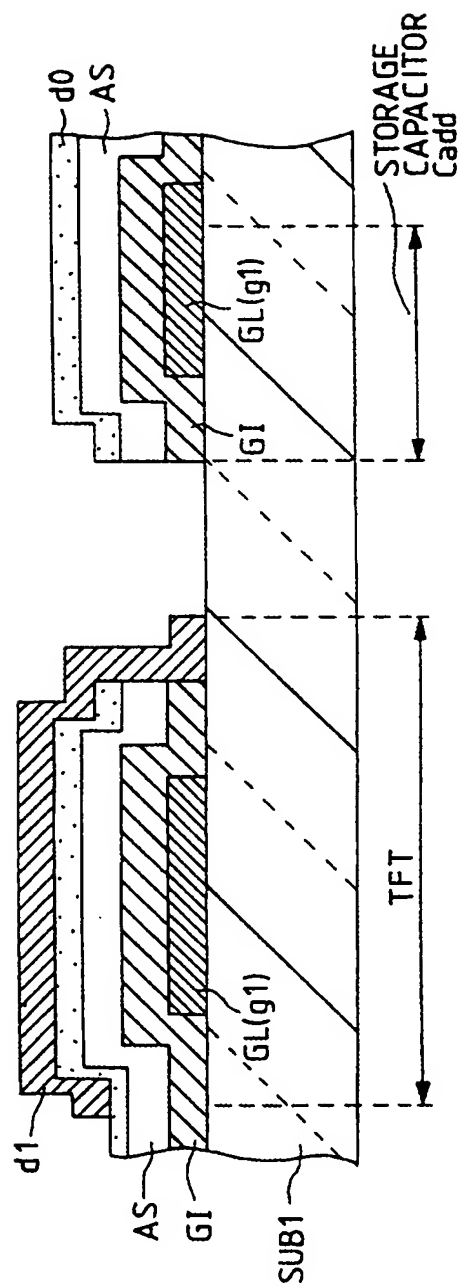


FIG. 14

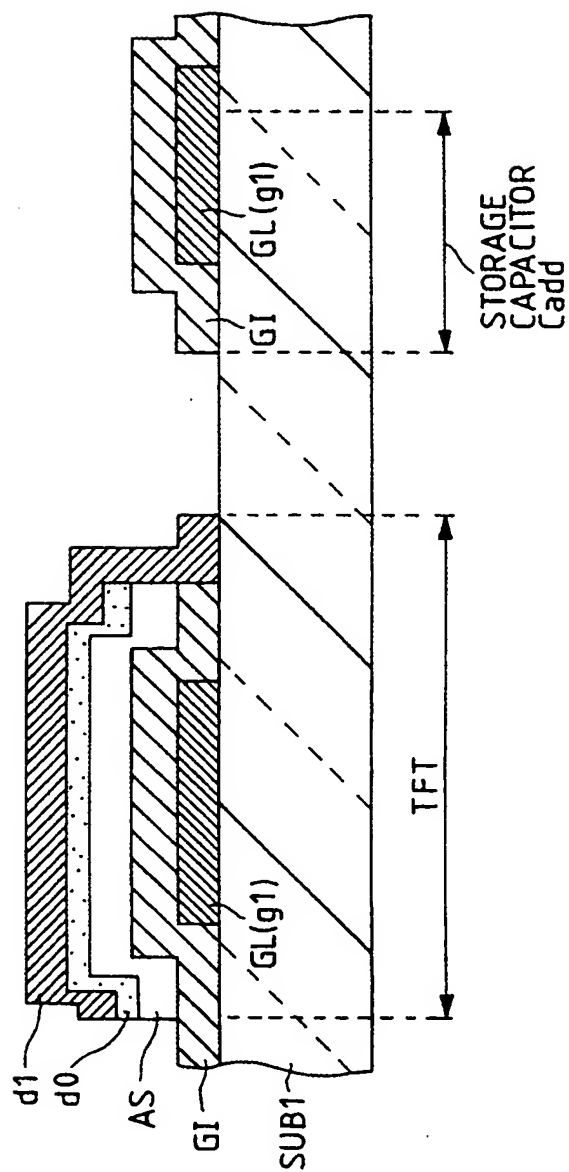


FIG. 15

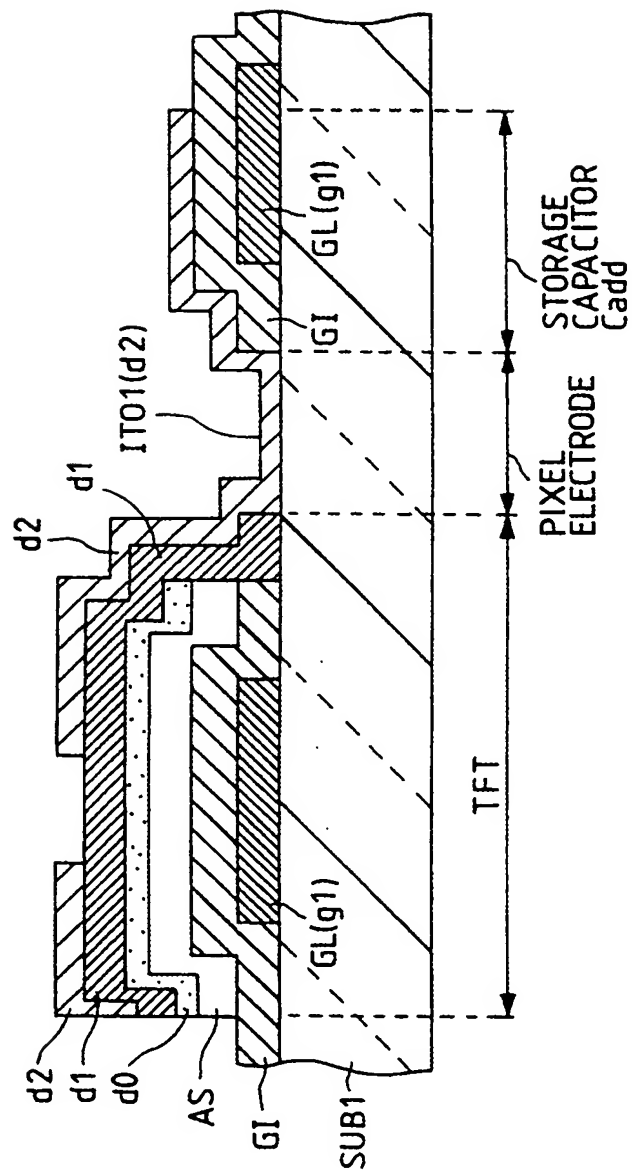


FIG. 16

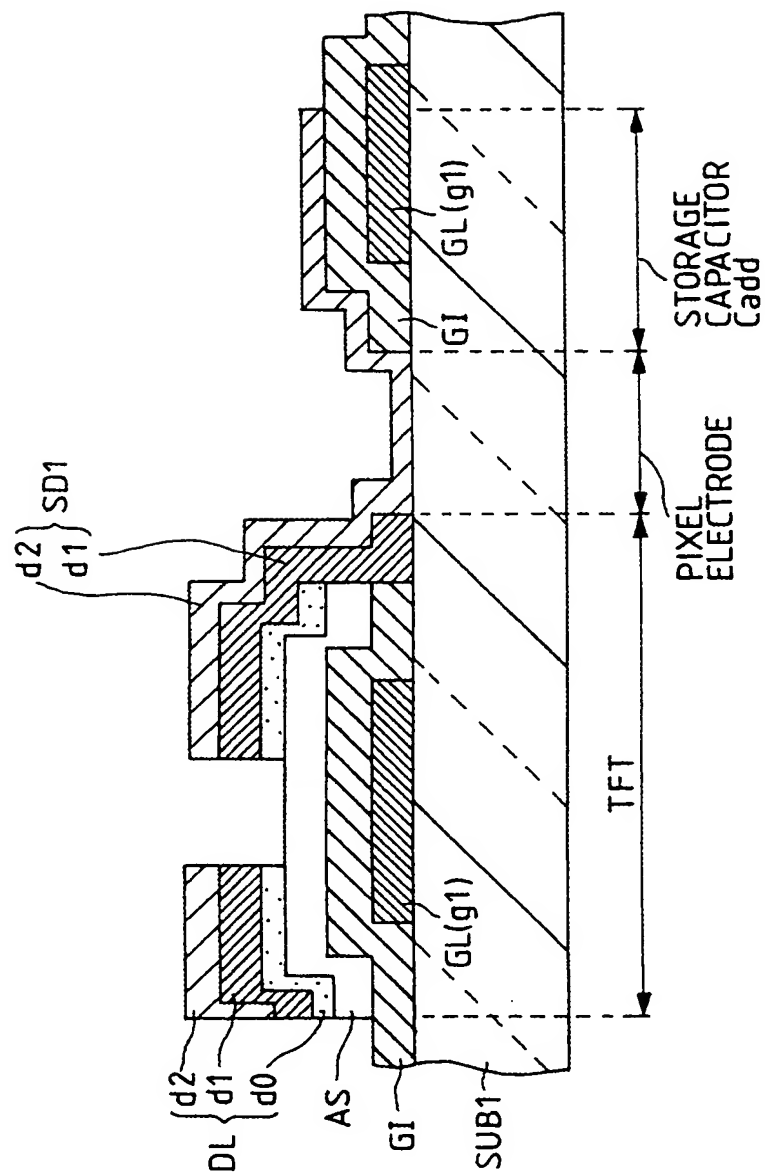


FIG. 17

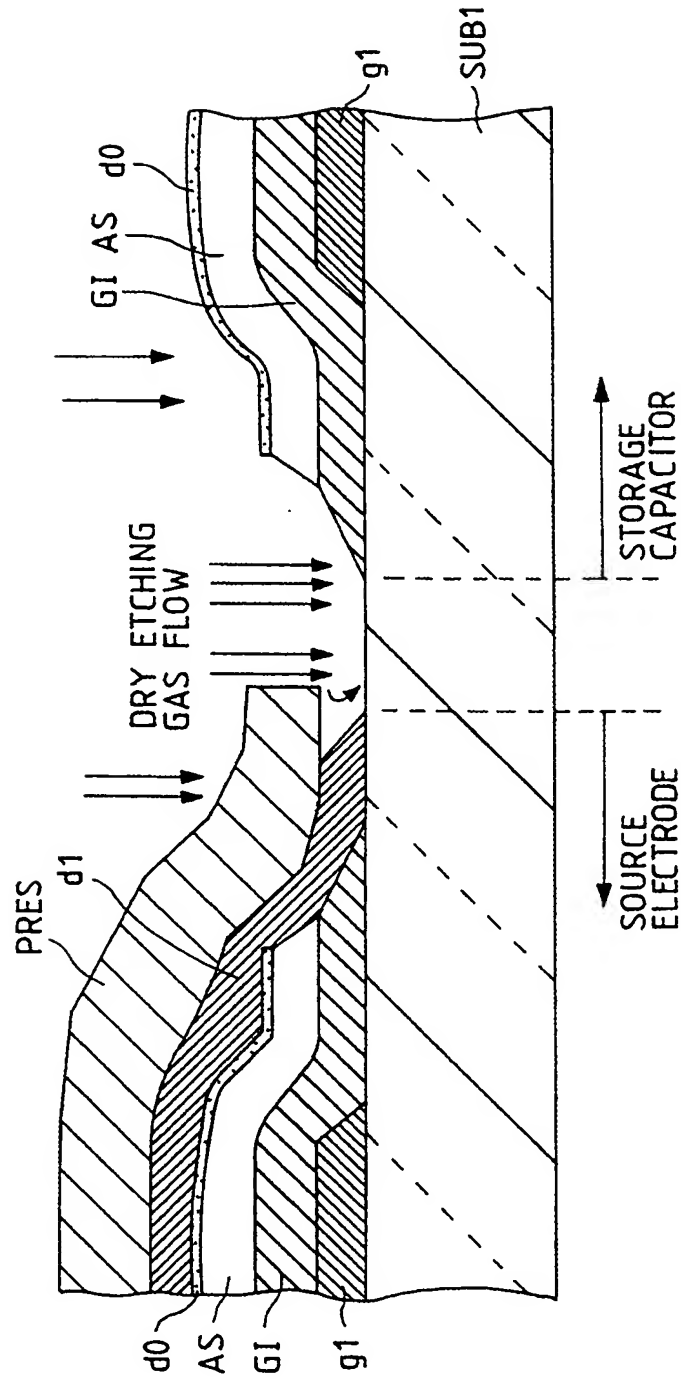


FIG. 18

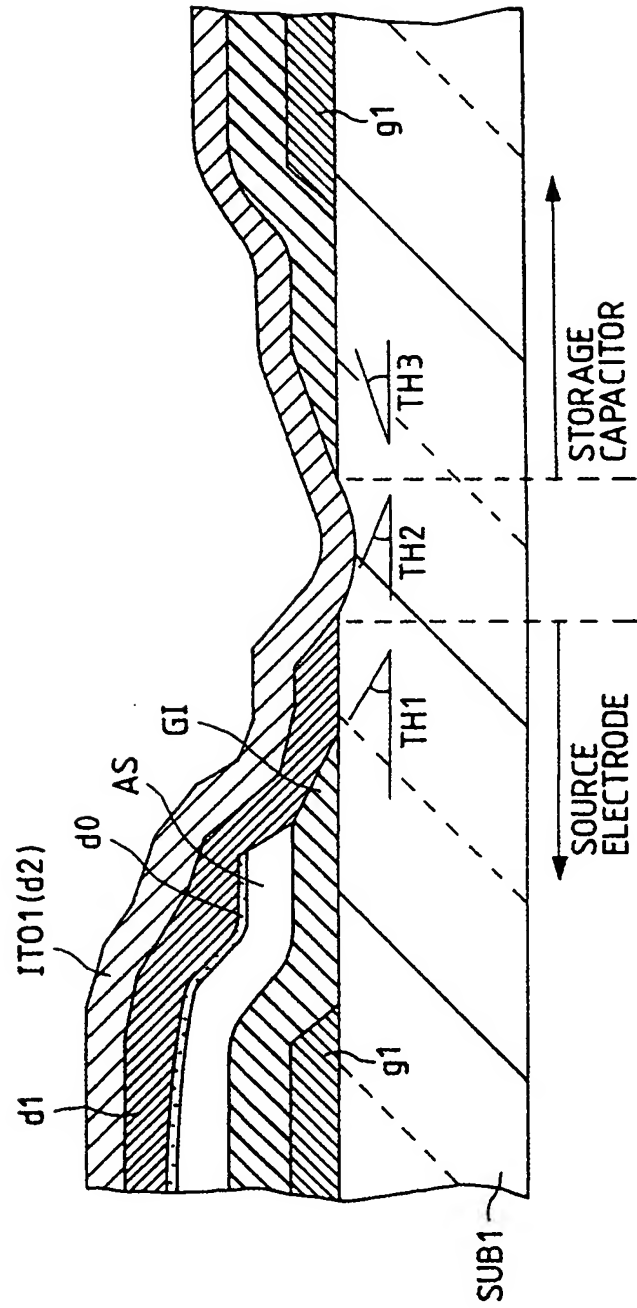


FIG. 19

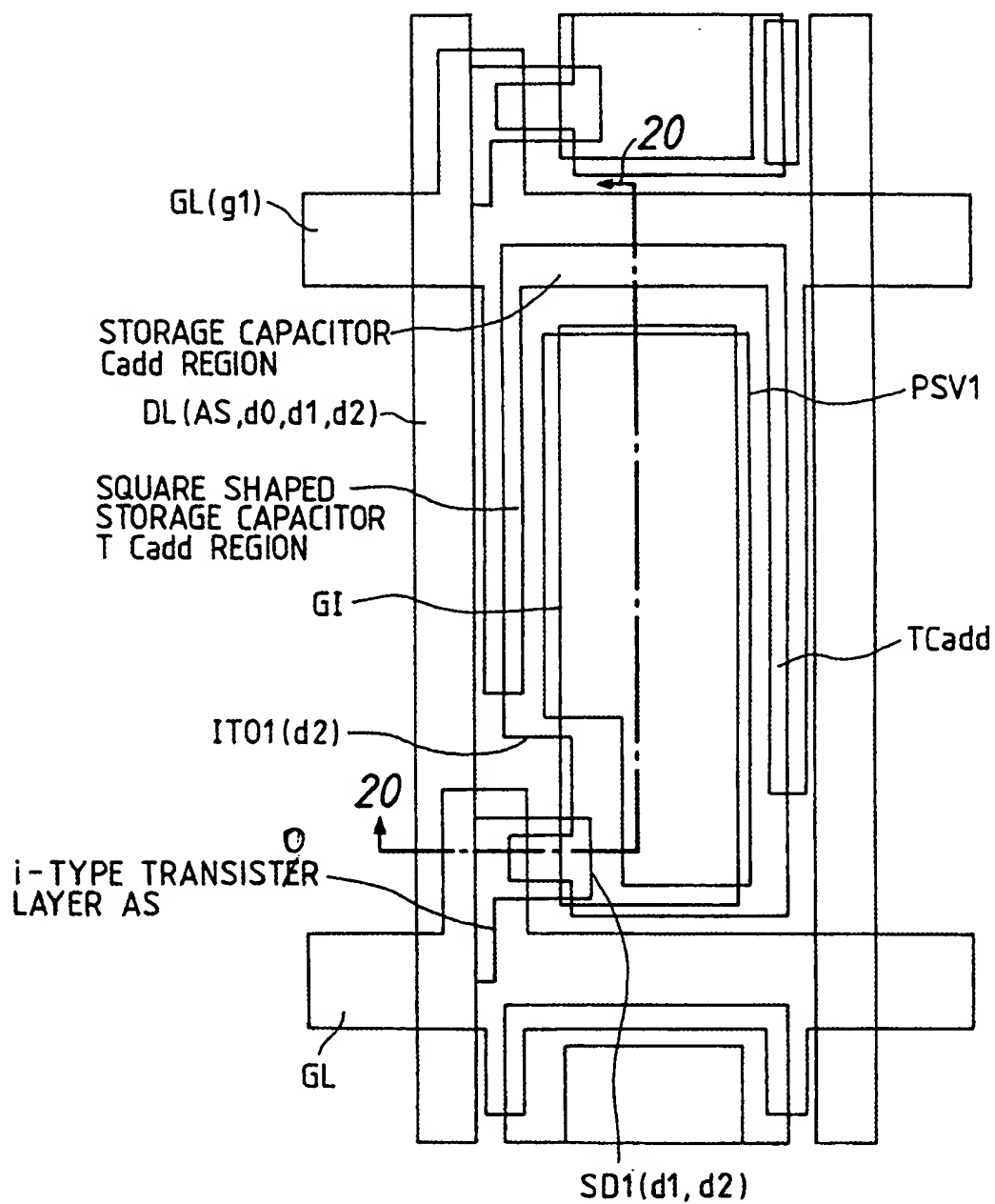


FIG. 20

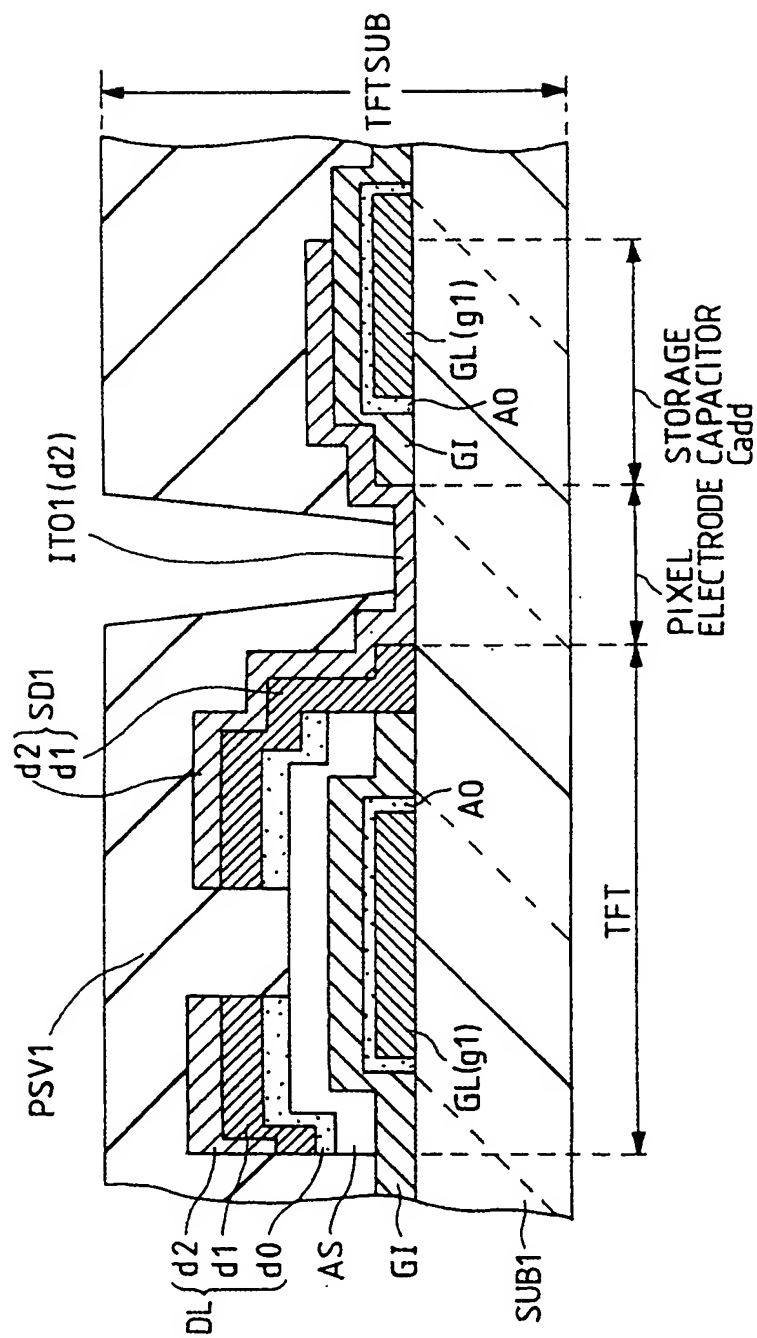


FIG. 21

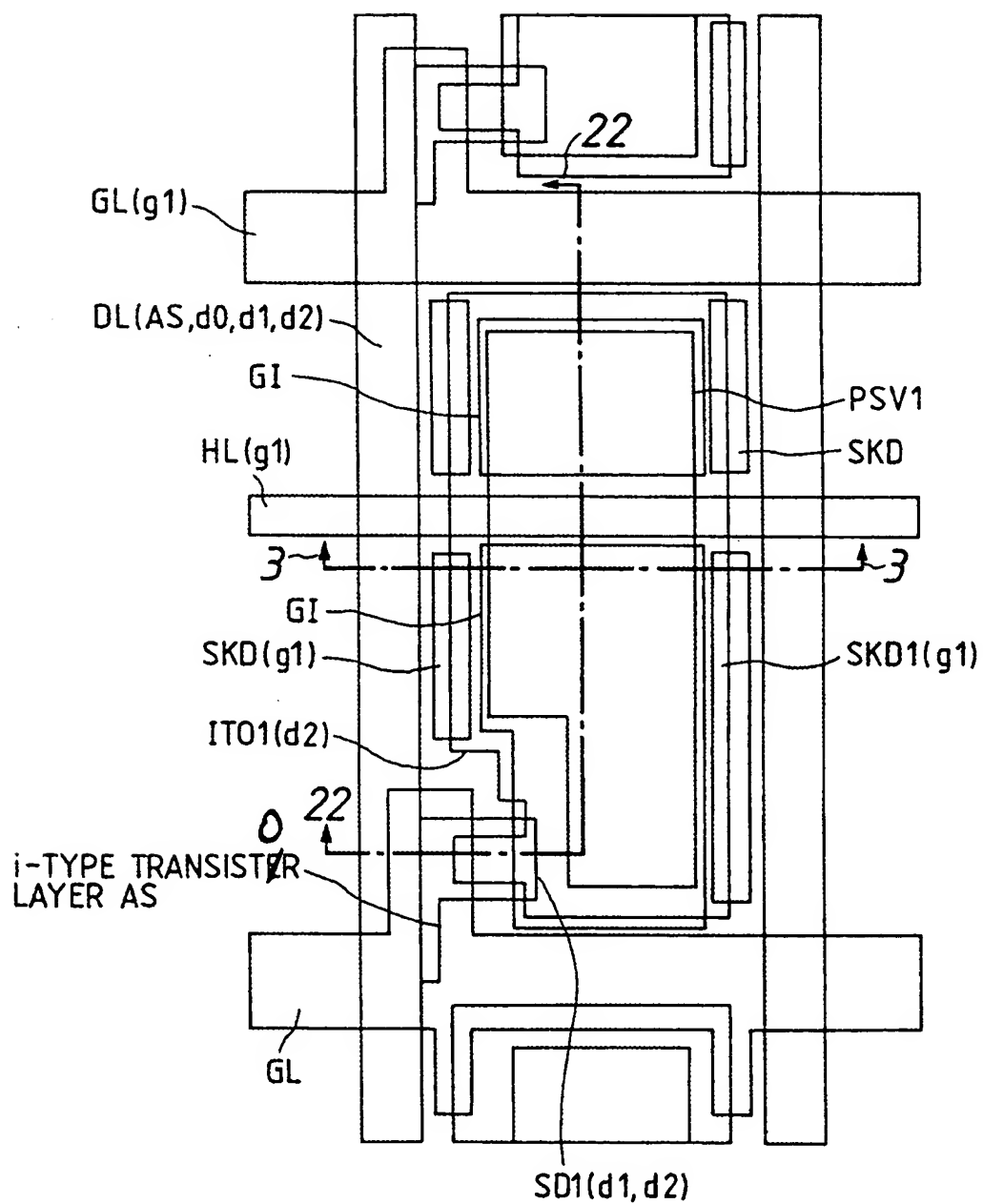


FIG. 22

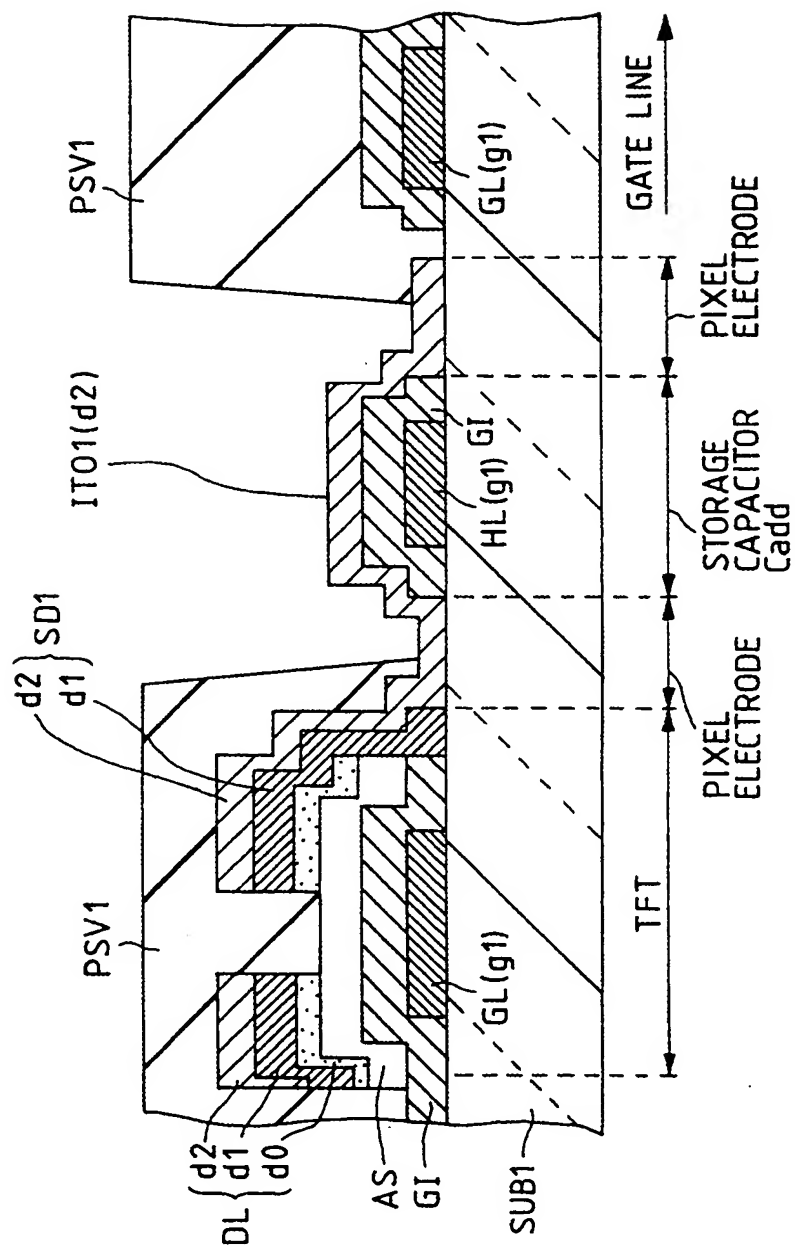


FIG. 23

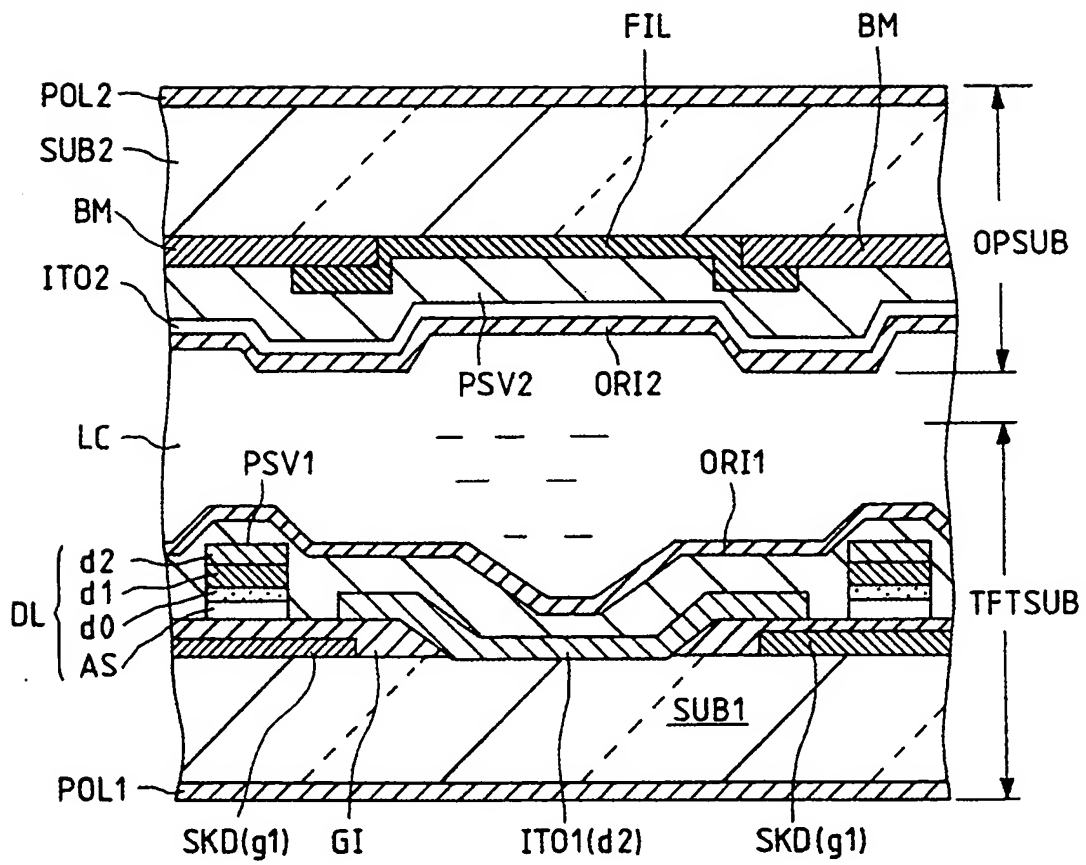


FIG. 24

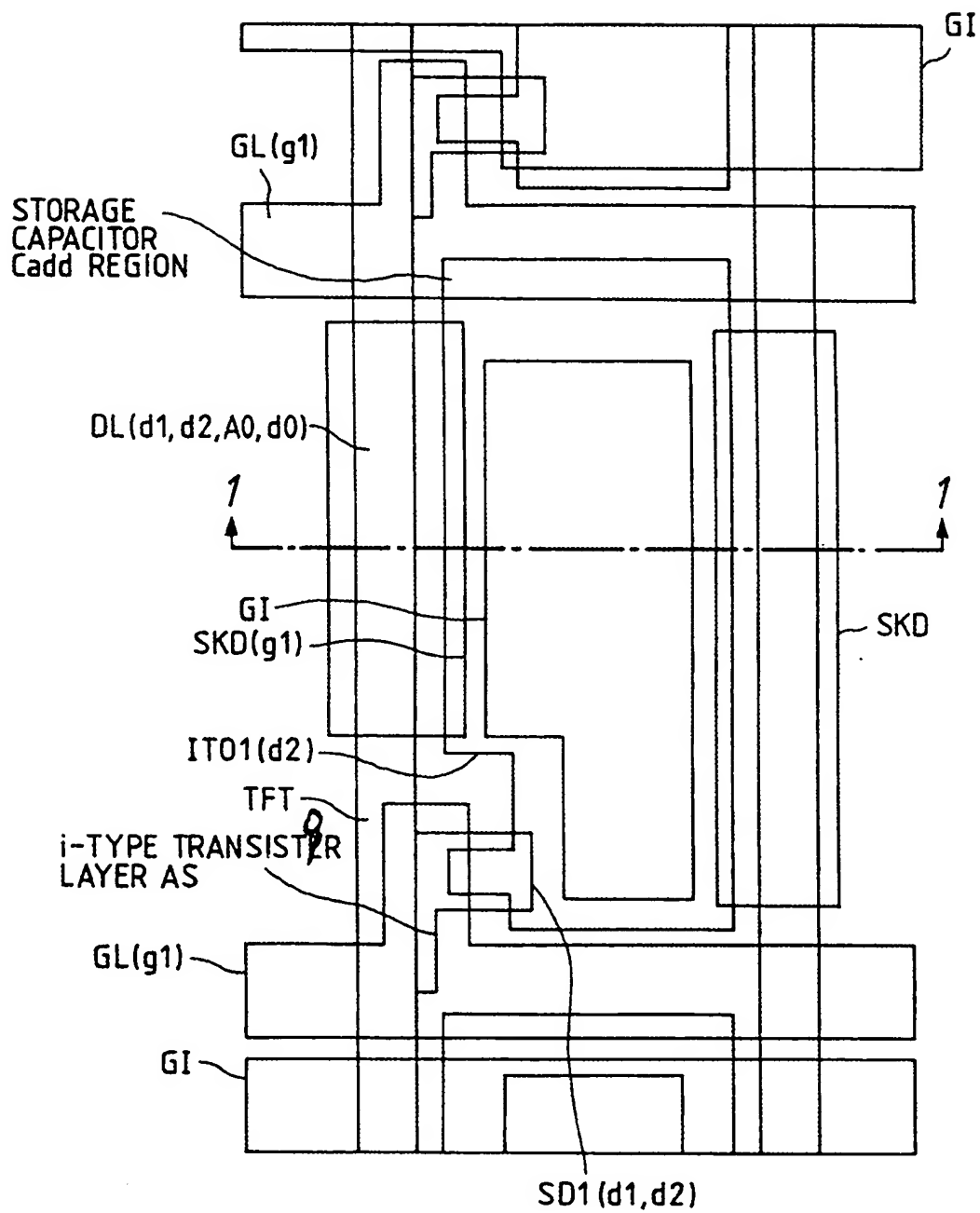


FIG. 25

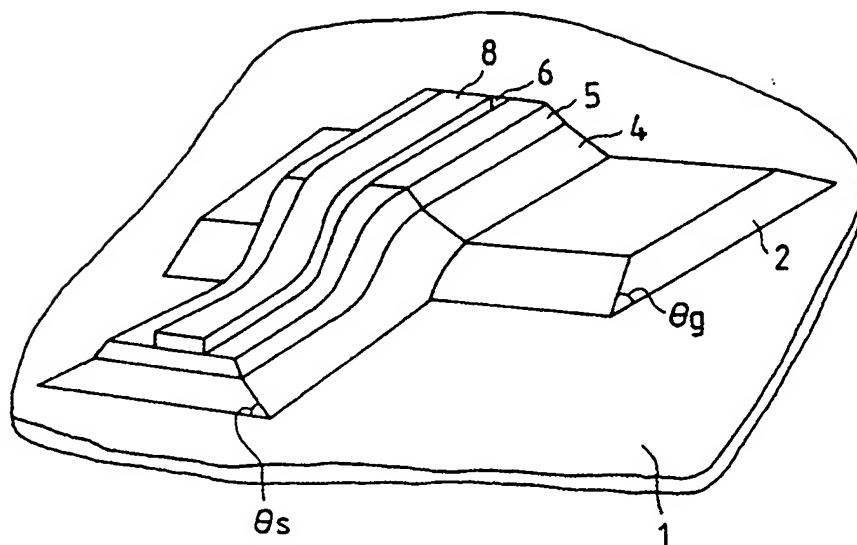
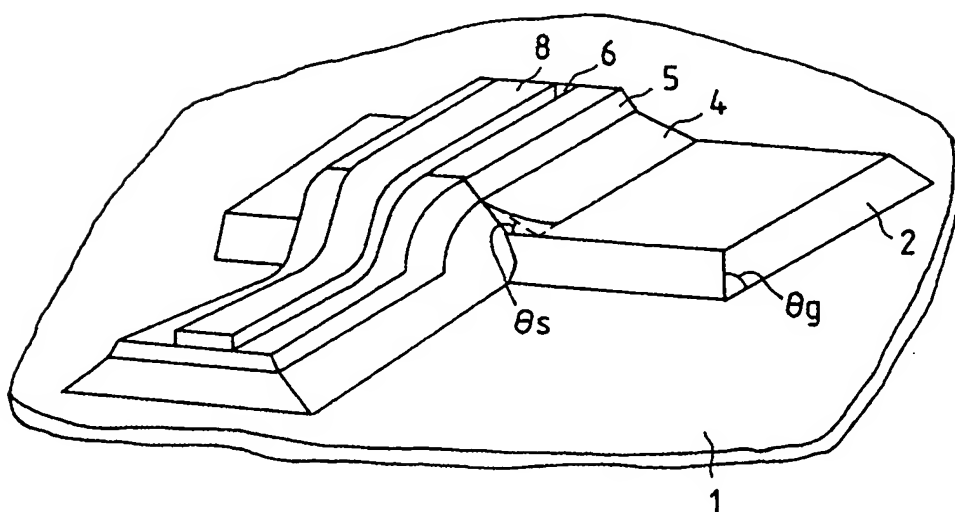


FIG. 27



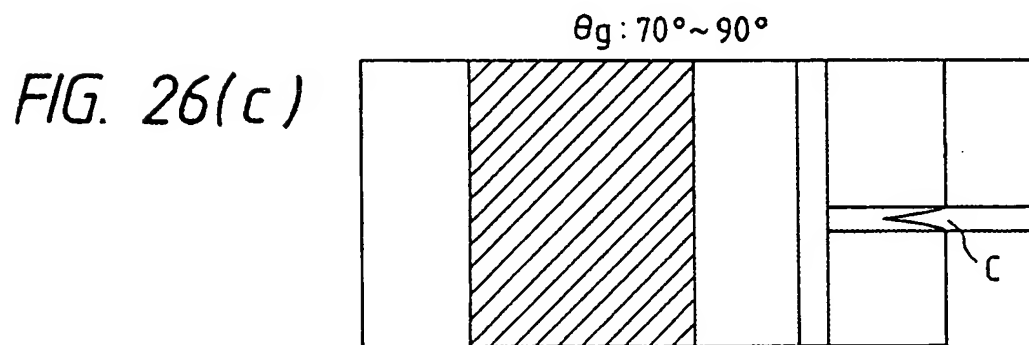
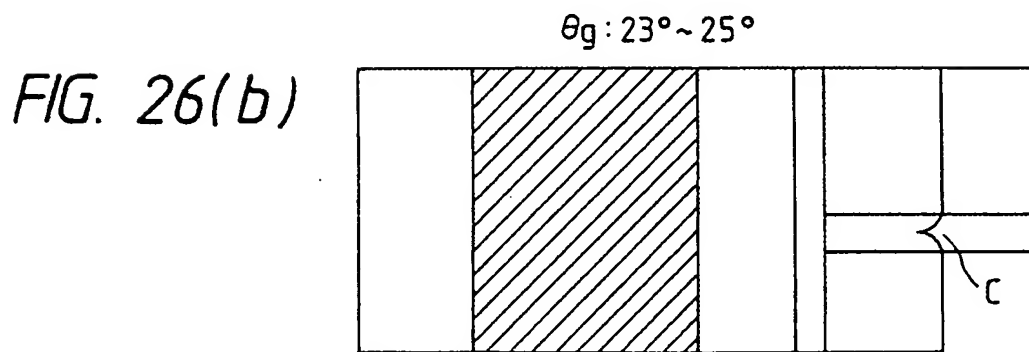
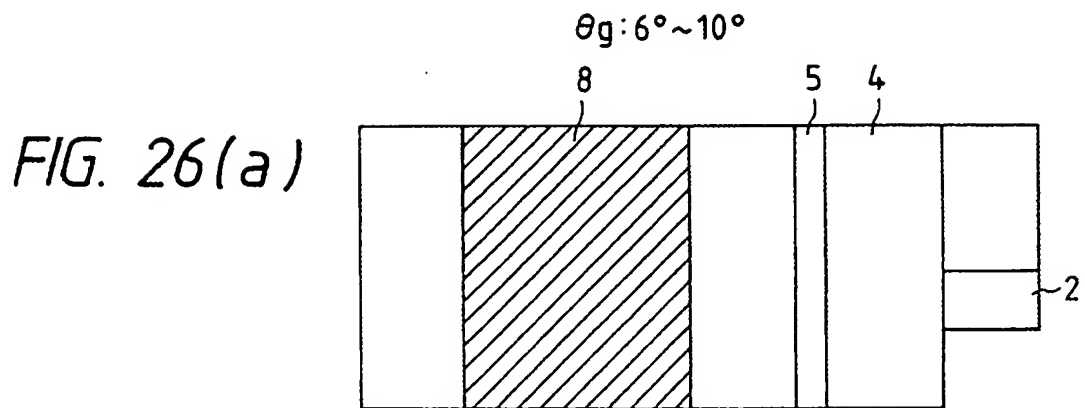


FIG. 28

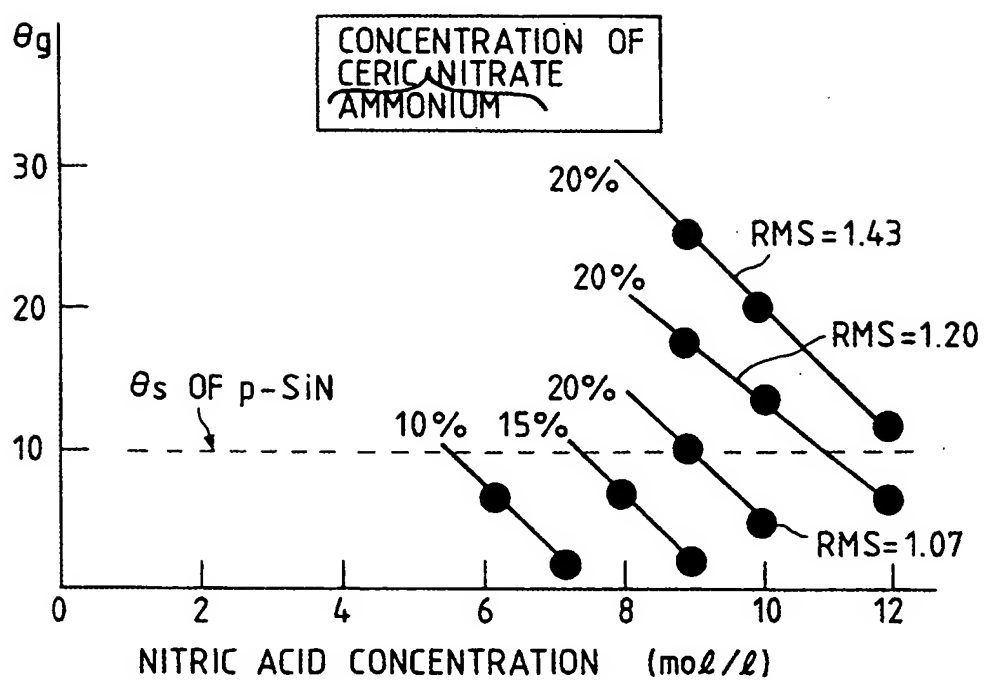


FIG. 29(a)

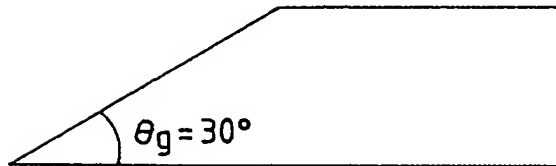
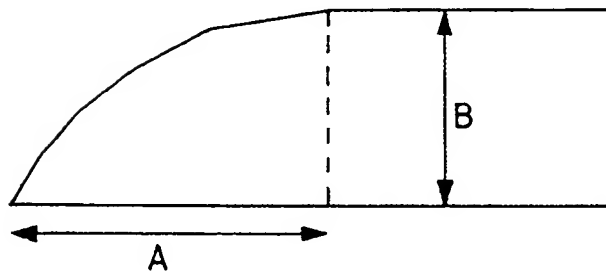
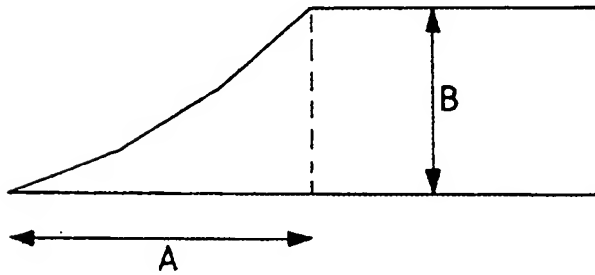


FIG. 29(b)



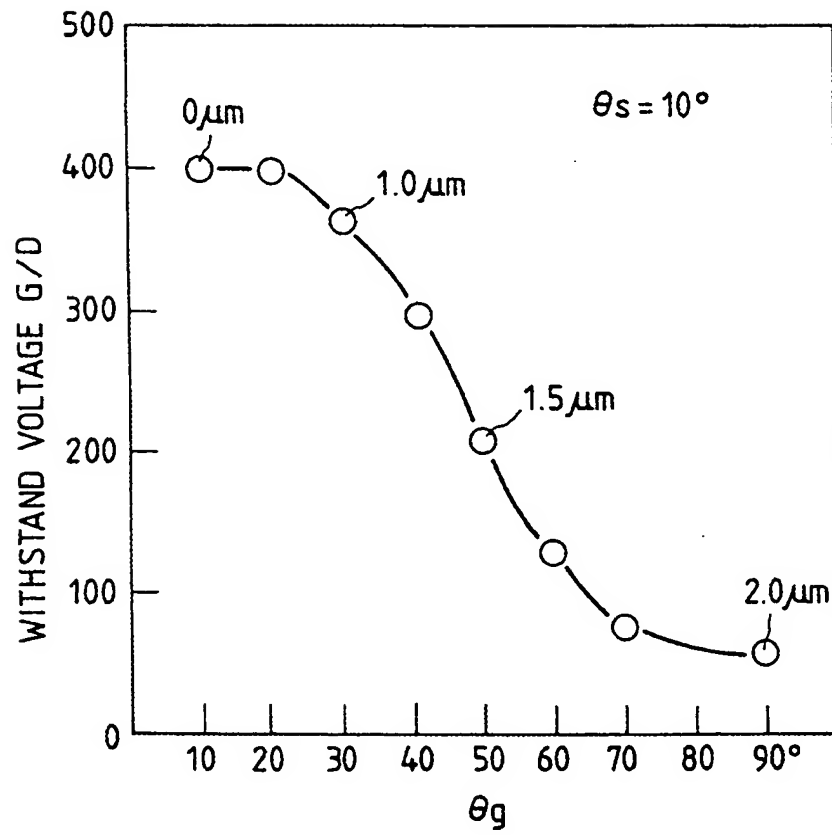
TAPER RATIO = B/A
= 0.62

FIG. 29(c)



TAPER RATIO = B/A
= 0.62

FIG. 30



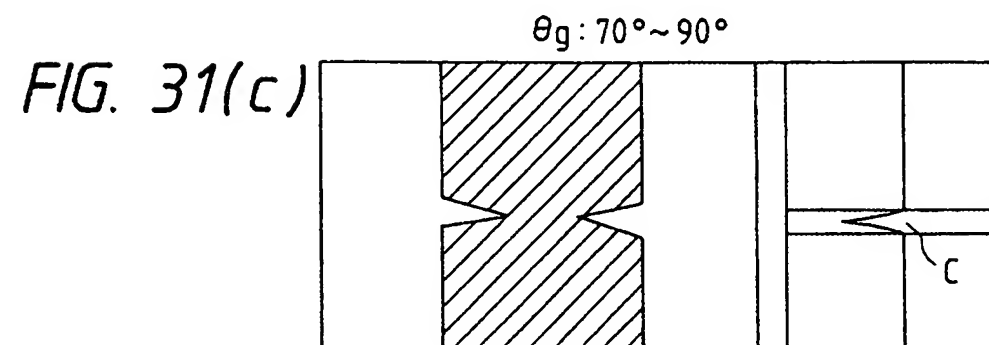
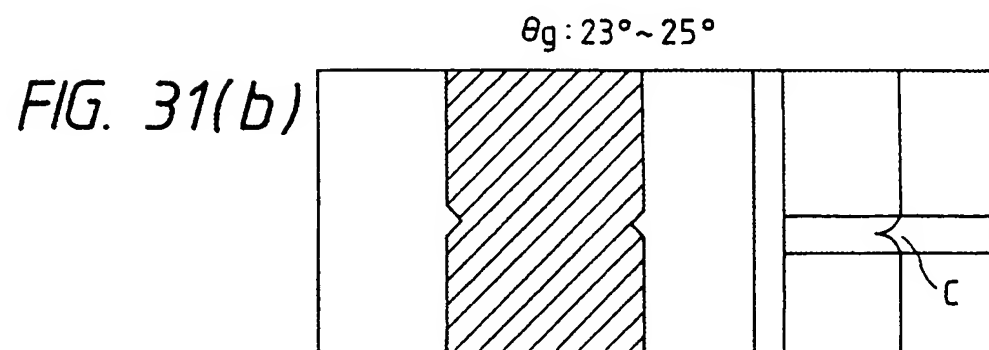
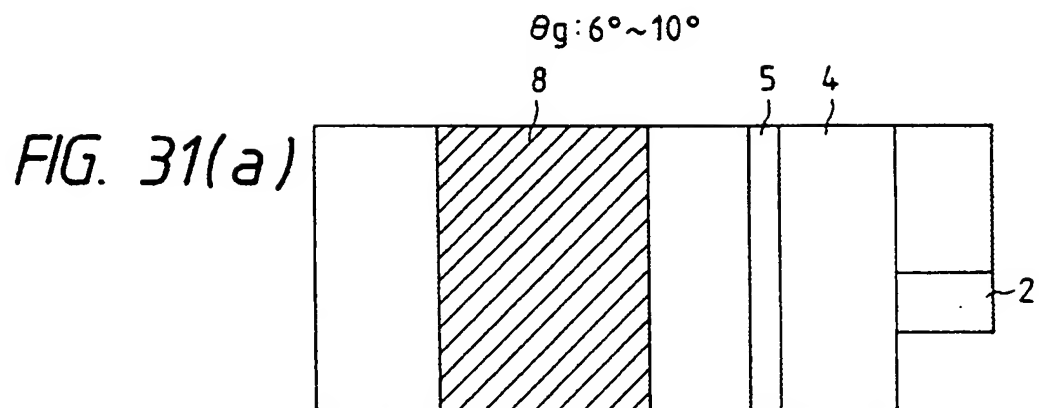


FIG. 32

